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T-52-33-55

Bus Controller for SAB 80286 Processors

SAB 82288

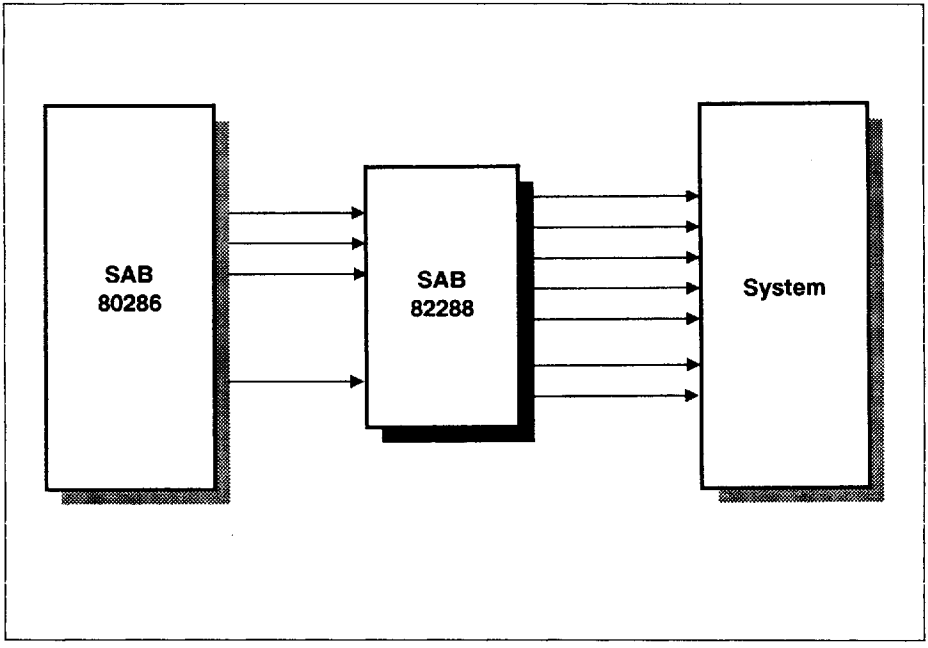
Preliminary

SAB 82288-6 up to 12 MHz
SAB 82288 up to 16 MHz

- Provides commands and control for local and system bus
- Offers wide flexibility in system configurations
- Flexible command timing

SAB 82288-1 up to 20 MHz

- Optimal Multibus®-compatible timing
- Control drivers with 16 mA I_{OL} and tristate command drivers with 32 mA I_{OL}
- Single +5V supply
- Plastic Package: P-DIP-20



The SAB 82288 bus controller is a 20-pin MYMOS component for use in SAB 80286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals.
Two modes of operation are possible: Multibus-compatible bus cycles, and high-speed bus cycles.

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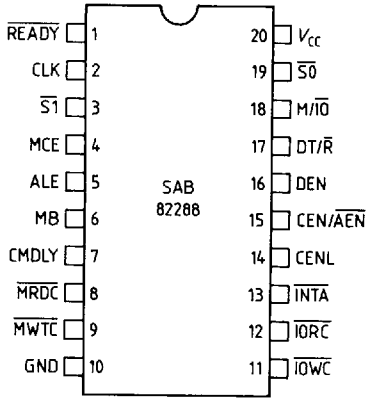
Ordering Information

Type	Ordering code	Package	Description
SAB 82288-P	Q67120-Y75	P-DIP-20	Bus controller up to 16 MHz
SAB 82288-6-P	Q67120-Y110	P-DIP-20	Bus controller up to 12 MHz
SAB 82288-1-P	Q67120-Y69	P-DIP-20	Bus controller up to 20 MHz

Pin Configuration
(P-DIP-20)



Pin Names

CLK	System Clock
$\overline{S0}$, $\overline{S1}$	Bus Cycle Status
M/$\overline{IO}$	Memory or I/O Select
MB	Multibus Mode Select
CENL	Command Enable Latched
CMDLY	Command Delay
$\overline{READY}$	Bus Cycle Termination
CEN/$\overline{AEN}$	Command Enable/Address Enable
ALE	Address Latch Enable
MCE	Master Cascade Enable
DEN	Data Enable
DT/$\overline{R}$	Data Transmit/Receive
$\overline{IOWC}$	I/O Write Command
$\overline{IORC}$	I/O Read Command
$\overline{MWTC}$	Memory Write Command
$\overline{MRDC}$	Memory Read Command
$\overline{INTA}$	Interrupt Acknowledge
V_{CC}	Power supply (+5 V)
GND	Ground (0 V)

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Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{READY}}$	1	I	**$\overline{\text{READY}}$** indicates the end of the current bus cycle. $\overline{\text{READY}}$ is an active low input. Multibus mode requires at least one wait state to allow the command outputs to become active. $\overline{\text{READY}}$ must be low during reset, to force the SAB 82288 into the idle state. Setup and hold times must be met for proper operation.
CLK	2	I	**SYSTEM CLOCK** provides the basic timing control for the SAB 82288 in an SAB 80286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and control outputs change.
$\overline{\text{S0}}$, $\overline{\text{S1}}$	3, 19	I	**BUS CYCLE STATUS** starts a bus cycle and, along with M/$\overline{\text{IO}}$, defines the type of bus cycle. These inputs are active low. A bus cycle is started when either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ is sampled low at the falling edge of CLK. These inputs have pullup resistors sufficient to hold them high when nothing drives them. Setup and hold times must be met for proper operation.

SAB 80286 bus cycle status definition

M/$\overline{\text{IO}}$	$\overline{\text{S1}}$	$\overline{\text{S0}}$	Type of bus cycle
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	None; idle
1	0	0	Halt or shutdown
1	0	1	Memory read
1	1	0	Memory write
1	1	1	None; idle

MCE	4	O	**MASTER CASCADE ENABLE** signals that a cascade address from a master SAB 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active high. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
ALE	5	O	**ADDRESS LATCH ENABLE** controls the address latches used to hold an address stable during a bus cycle. This control output is active high. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MB	6	I	**MULTIBUS MODE SELECT** determines timing of the command and control outputs. When high, the bus controller operates in Multibus mode. When low, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{\text{AEN}}$ input pin is selected by this signal. Typically, this input is a strapping option and not dynamically changed. This input may be connected to V_{CC} or GND.

Pin Definitions and Function (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CMDLY	7	I	**COMMAND DELAY** allows delaying the start of a command. CMDLY is an active high input. If sampled high, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled low the selected command is enabled. If $\overline{\text{READY}}$ is detected low before the command output is activated, the SAB 82288 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command.
$\overline{\text{MRDC}}$	8	O	**$\overline{\text{MEMORY READ COMMAND}}$** instructs the memory device to place data onto the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{MWTC}}$	9	O	**$\overline{\text{MEMORY WRITE COMMAND}}$** instructs a memory device to read the data on the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{IOWC}}$	11	O	**$\overline{\text{I/O WRITE COMMAND}}$** instructs an I/O device to read the data on the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{IORC}}$	12	O	**$\overline{\text{I/O READ COMMAND}}$** instructs an I/O device to place data onto the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{INTA}}$	13	O	**$\overline{\text{INTERRUPT ACKNOWLEDGE}}$** tells an interrupting device that its interrupt request is being acknowledged. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
CENL	14	I	**COMMAND ENABLE LATCHED** is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active high input latched internally at the start of each bus cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to V_{CC} to select this SAB 82288 for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.

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Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CEN/$\overline{AEN}$	15	I	**COMMAND ENABLE/$\overline{\text{ADDRESS ENABLE}}$** controls the command and DEN outputs of the bus controller. CEN/$\overline{AEN}$ inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to V_{CC} or GND. When MB is high this pin has the $\overline{AEN}$ function. $\overline{AEN}$ is an active low input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit tristate off and become inactive (high). $\overline{AEN}$ high indicates that the CPU does not have control of the shared bus and forces the command outputs into tristate off and DEN inactive (low). $\overline{AEN}$ would normally be controlled by an SAB 82289 bus arbiter which activates $\overline{AEN}$ when that arbiter owns the bus to which the bus controller is attached. When MB is low this pin has the CEN function. CEN is an unlatched active high input which allows the bus controller activate its command and DEN outputs. With MB low, CEN low forces the command and DEN outputs inactive but does not tristate them.
DEN	16	O	**DATA ENABLE** controls when data transceivers connected to the local data bus should be enabled. DEN is an active high control output. DEN is delayed for write cycles in the Multibus mode.
DT/$\overline{R}$	17	O	**DATA TRANSMIT/$\overline{\text{RECEIVE}}$** establishes the direction of data flow to or from the local data bus. When high, this control output indicates that a write bus cycle is being performed. A low indicates a read bus cycle. DEN is always inactive when DT/$\overline{R}$ changes states. This output is high when no bus cycle is active. DT/$\overline{R}$ is not affected by any of the control inputs.
M/$\overline{IO}$	18	I	**MEMORY or $\overline{\text{I/O}}$** SELECT determines whether the current bus cycle is in the memory space or I/O space. When low, the current bus cycle is in the I/O space. This input has a pullup resistor sufficient to hold it high when nothing drives it. Setup and hold times must be met for proper operation.
V_{CC}	20	–	**POWER SUPPLY** (+5V)
GND	10	–	**GROUND** (0V)

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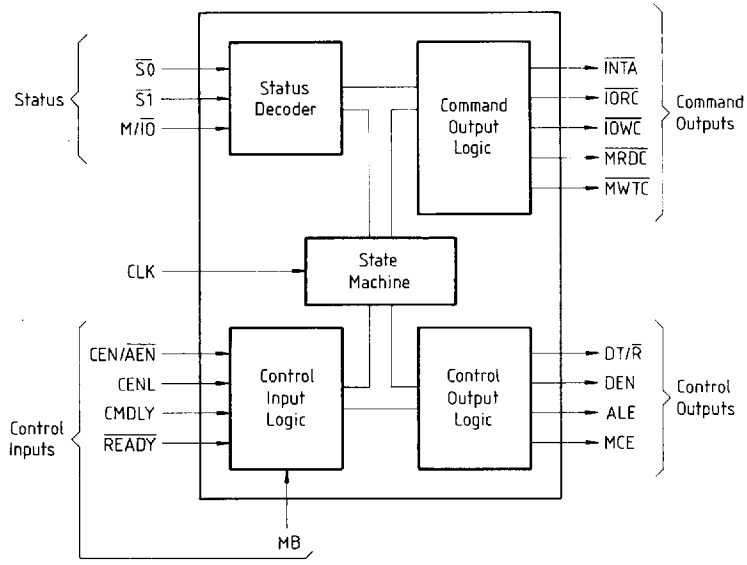
Block Diagram



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Functional Description

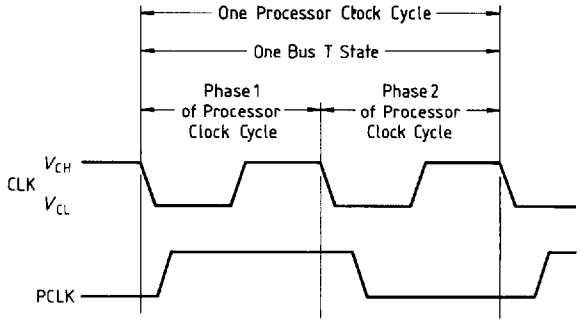
Introduction

The SAB 82288 bus controller is used in SAB 80286 systems to provide address latch control, data transceiver control, and standard level-type command outputs. The command outputs are timed and have sufficient drive capabilities for large TTL buses and meet all IEEE-796 requirements for Multibus. A special Multibus mode is provided to statisfy all address/data setup and hold time requirements. Command timing may be tailored to special needs via a CMDLY input to determine the start of a command and $\overline{\text{READY}}$ to determine the end of a command.
Connection to multiple buses is supported with a latched enable input (CENL). An address decoder can determine which, if any, bus controller should be enabled for the bus cycle. This input is latched to allow an address decoder to take full advantage of the pipelined timing on the SAB 80286 local bus.
Buses shared by several bus controllers are supported. An $\overline{\text{AEN}}$ input prevents the bus controller from driving the shared bus command and data signals except when enabled by an external bus arbiter such as the SAB 82289.
Separate DEN and DT/$\overline{\text{R}}$ outputs control the data transceivers for all buses. Bus contention is eliminated by disabling DEN before changing DT/$\overline{\text{R}}$. The DEN timing allows sufficient time for tristate bus drivers to enter tristate off before enabling other drivers onto the same bus.
The term CPU refers to any SAB 80286 processor or SAB 80286 support component which may become an SAB 80286 local bus master and thereby drive the SAB 82288 status inputs.

Processor Cycle Definition

Any CPU which drives the local bus uses an internal clock which is one half the frequency of the system clock (CLK) (see figure below). Knowledge of the phase of the local bus master's internal clock is required for proper operation of the SAB 80286 local bus. The local bus master informs the bus controller of its internal clock phase when it asserts the status signals. Status signals are always asserted in phase 1 of the local bus master's internal clock.

CLK Relationship to the Processor Clock and Bus T-States



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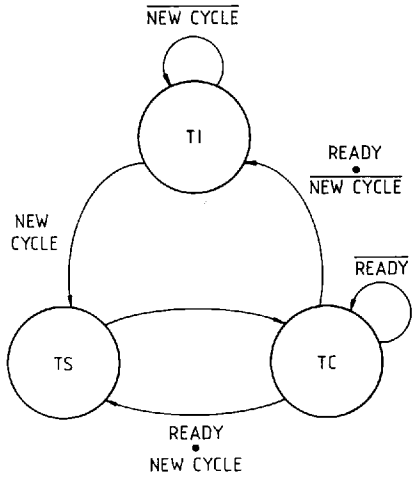
Bus State Definition

The SAB 82288 bus controller has three bus states (see figure below): Idle (TI), Status (TS), and Command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU processor clock phases.
The TI bus state occurs when no bus cycle is currently active on the SAB 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the TI state.

Bus States



Bus Cycle Definition

The $\overline{S1}$ and $\overline{S0}$ inputs signal the start of a bus cycle. When either input becomes low, a bus cycle is started. The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ is active (see figure on bus cycle definition). These inputs are sampled by the SAB 82288 at every falling edge of CLK. When either $\overline{S1}$ or $\overline{S0}$ is sampled low, the next CLK cycle is considered the second phase of the internal CPU clock cycle.
The local bus enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state is called a wait state.
The $\overline{READY}$ input determines whether the current TC bus state is to be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each TC bus state to see if it is active. If sampled high, the TC bus state is repeated. This is called inserting a wait state. The control and command outputs do not change during wait states. When $\overline{READY}$ is sampled low, the current bus cycle is terminated. Note that the bus controller may enter the TS bus state directly from TC if the status lines are sampled active at the next falling edge of CLK.

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Bus Cycle Definition

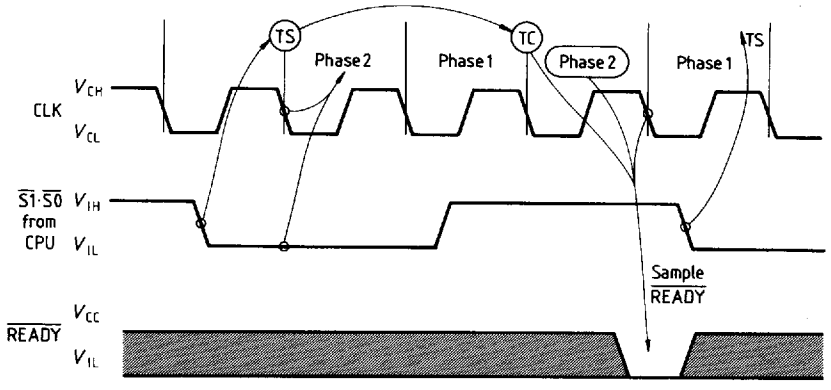

Table 2
Command and Control Output for Each Type of Bus Cycle

Type of bus cycle	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Command activated	DT/$\overline{R}$ state	ALE, DEN issued?	MCE issued?
Interrupt acknowledge	0	0	0	$\overline{INTA}$	low	yes	yes
I/O read	0	0	1	$\overline{IORC}$	low	yes	no
I/O write	0	1	0	$\overline{IOWC}$	high	yes	no
None; idle	0	1	1	none	high	no	no
Halt/shutdown	1	0	0	none	high	no	no
Memory read	1	0	1	$\overline{MRDC}$	low	yes	no
Memory write	1	1	0	$\overline{MWTC}$	high	yes	no
None; idle	1	1	1	none	high	no	no

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Operating Modes

Two types of buses are supported by the SAB 82288: Multibus and non-Multibus. When the MB input is high, Multibus timing is used. In Multibus mode, the SAB 82288 delays command and data activation to meet IEEE-796 requirements on address to command active and write data to command active setup timing. Multibus mode requires at least one wait state in the bus cycle since the command outputs are delayed. The non-Multibus mode does not delay any outputs and does not require wait states. The MB input affects the timing of the command and DEN outputs.

Command and Control Outputs

The type of bus cycle performed by the local bus master is encoded in the M/$\overline{IO}$, $\overline{S1}$, and $\overline{S0}$ inputs. Different command and control outputs are activated depending on the type of bus cycle. Table 2 indicates the cycle decoding done by the SAB 82288 and the effect on command, DT/$\overline{R}$, ALE, DEN, and MCE outputs.
Bus cycles come in three forms: read, write, and halt. Read bus cycles include memory read, I/O read, and interrupt acknowledge. The timing of the associated read command outputs ($\overline{MRDC}$, $\overline{IORC}$, and $\overline{INTA}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical for all read bus cycles. Read cycles differ only in which command output is activated. The MCE control output is only asserted during interrupt acknowledge cycles.
Write bus cycles activate different control and command outputs with different timing than read bus cycles. Memory write and I/O write are write bus cycles whose timing for command outputs ($\overline{MWTC}$ and $\overline{IOWC}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical. They differ only in which command output is activated.
Halt bus cycles are different because no command or control output is activated. All control inputs are ignored until the next bus cycle is started via $\overline{S1}$ and $\overline{S0}$.
The basic command and control output timing for read and write bus cycles is shown in the next five figures. Halt bus cycles are not shown since they activate no outputs. The basic idle-read-idle and idle-write-idle bus cycles are shown. The signal label $\overline{CMD}$ represents the appropriate command output for the bus cycle. For those five figures, the CMDLY input is connected to GND and CENL to V_{CC}. The effects of CENL and CMDLY are described later in the section on control inputs.
The next two figures show non-Multibus cycles. MB is connected to GND while CEN is connected to V_{CC}. The figure on page 11 shows a read cycle with no wait states while the figure on page 12 shows a write cycle with one wait state. The $\overline{READY}$ input is shown to illustrate how wait states are added.

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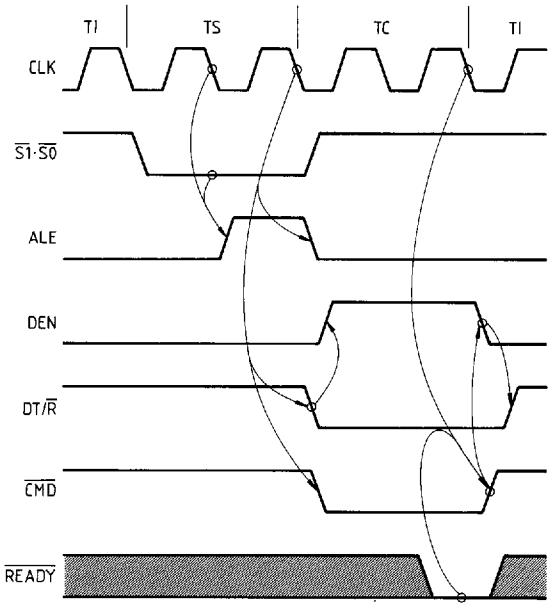
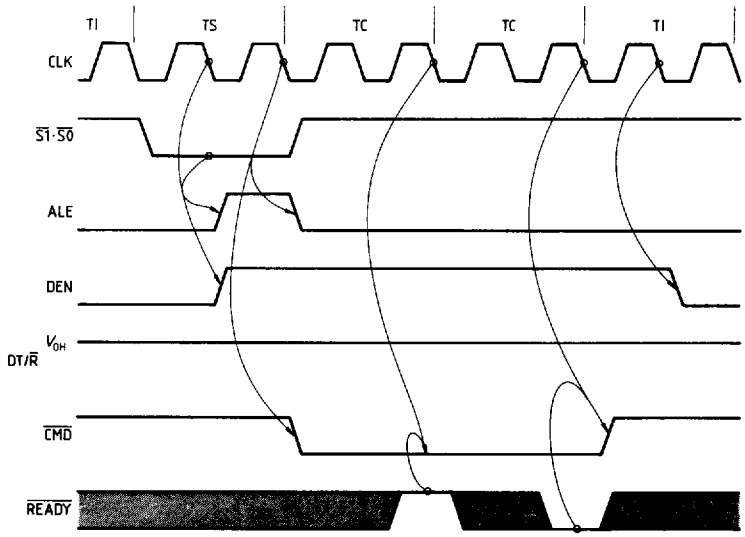
Idle-Read-Idle Bus Cycles with MB = 0



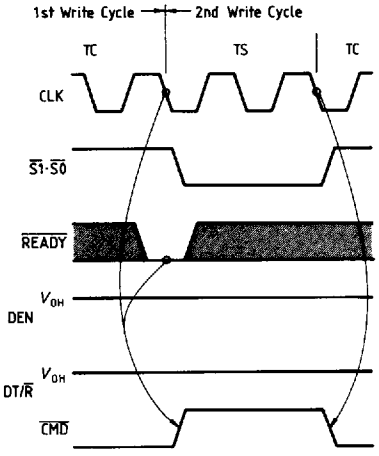
Bus cycles can occur back-to-back with no TI bus states between TC and TS. Back-to-back cycles do not affect the timing of the command and control outputs. Command and control outputs always reach the states shown for the same clock edge (within TS, TC, or following bus state) of a bus cycle. A special case in control timing occurs for back-to-back write cycles with MB = 0. In this case, DT/$\overline{R}$ and DEN remain high between the bus cycles (see respective write-write cycle diagram). The command and ALE output timing does not change.

The figures on pages 13 and 14 show a Multibus cycle with MB = 1. $\overline{AEN}$ and CMDLY are connected to GND. The effects of CMDLY and $\overline{AEN}$ are described later in the section on control inputs. The top figure shows a read cycle with one wait state and the figure below shows a write cycle with two wait states. The second wait state of the write cycle is shown only for example purposes and is not required. The $\overline{READY}$ input is shown to illustrate how wait states are added.

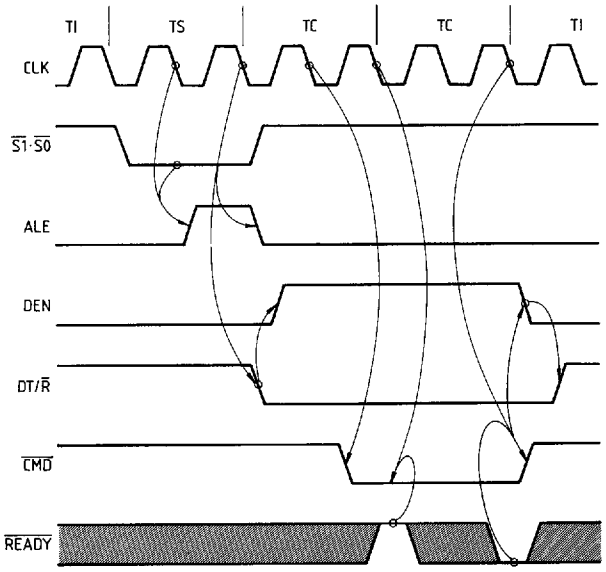
Idle-Write-Idle Bus Cycles with MB = 0



Write-Write Bus Cycles with MB = 0



Idle-Read-Idle Bus Cycles with MB = 1



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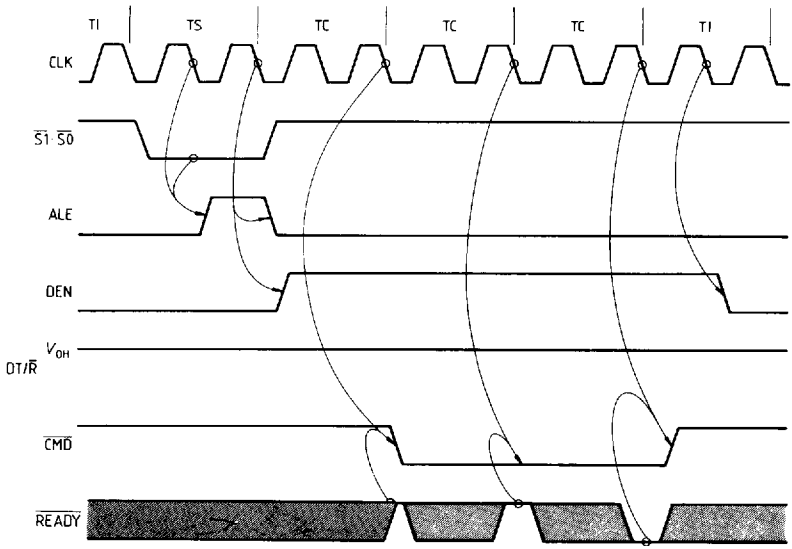
Idle-Write-Idle Bus Cycles with MB = 1



The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus mode to satisfy three requirements:

1) 50 ns minimum setup time for valid address before any command output becomes active.
2) 50 ns minimum setup time for valid write data before any write command output becomes active.
3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach tristate off.

Three signal transitions are delayed by MB = 1 as compared to MB = 0:

1) The high to low transition of the read command outputs ($\overline{IORC}$, $\overline{MRDC}$, and $\overline{INTA}$) is delayed one CLK cycle.
2) The high to low transition of the write command outputs ($\overline{IOWC}$ and $\overline{MWTC}$) is delayed two CLK cycles.
3) The low to high transition of DEN for write cycles is delayed one CLK cycle.

Back-to-back bus cycles with MB = 1 do not change the timing of any of the command or control outputs. DEN always becomes inactive between bus cycles with MB = 1.

Except for a halt or shutdown bus cycle, ALE will be issued during the second half of TS for any bus cycle. ALE becomes inactive at the end of the TS to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during phase 2 of any TC bus state. ALE is not affected by any control input.

The following figure shows how MCE is timed during interrupt acknowledge (INTA) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master SAB 8259A valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing with a read bus cycle. MCE is not affected by any control input.

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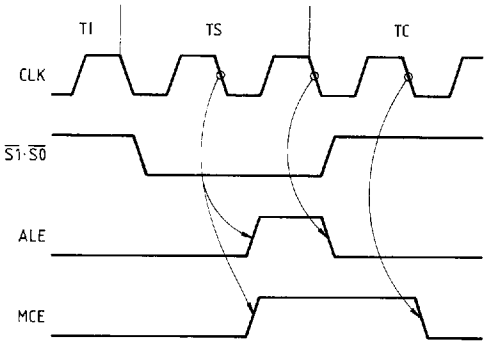
MCE Operation for an INTA Bus Cycle



Control Inputs

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. For many SAB 80286 systems, each CPU will have more than one bus which may be used to perform a bus cycle. Normally, a CPU will only have one bus controller active for each bus cycle. Some buses may be shared by more than one CPU (i.e. Multibus) requiring only one of them use the bus at a time.

Systems with multiple and shared buses use two control input signals of the SAB 82288 bus controller, CENL and $\overline{AEN}$ (see figure on system use of those signals). CENL enables the bus controller to control the current bus cycle. The $\overline{AEN}$ input prevents a bus controller from driving its command outputs. $\overline{AEN}$ high means that another bus controller may be driving the shared bus.

In the figure on the $\overline{AEN}$ and CENL signal, two buses are shown: a local bus and a Multibus. Only one bus is used for each CPU bus cycle. The CENL inputs of the bus controllers select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The SAB 82288 connected to the shared Multibus must be selected by CENL and be given access to the Multibus by $\overline{AEN}$ before it will begin a Multibus operation.

CENL must be sampled high at the end of the TS bus state (see waveforms) to enable the bus controller to activate its command and control outputs. If sampled low the commands and DEN will not go active and DT/$\overline{R}$ will remain high. The bus controller will ignore the CMDLY, CEN, and $\overline{READY}$ inputs until another bus cycle is started via $\overline{S1}$ and $\overline{S0}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched to avoid the need for latching its input.

The CENL input can effect the DEN control output.
When MB = 0, DEN normally becomes active during phase 2 of TS in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled low, the DEN output will be forced low during TC as shown in the timing waveforms.

When MB = 1, CEN/$\overline{\text{AEN}}$ becomes $\overline{\text{AEN}}$, $\overline{\text{AEN}}$ controls when the bus controller command outputs enter and exit tristate off. $\overline{\text{AEN}}$ is intended to be driven by a bus arbiter, like the SAB 82289, which assures only one bus controller is driving the shared bus at any time. When $\overline{\text{AEN}}$ makes a low to high transition, the command outputs immediately enter tristate off and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into tristate off (see next figure). The low to high transition of $\overline{\text{AEN}}$ should only occur during TI or TS bus states.

The high-to-low transition of $\overline{\text{AEN}}$ signals that the bus controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, $\overline{\text{AEN}}$ can become active during any T-state. $\overline{\text{AEN}}$ low immediately allows DEN to go to the appropriate state. Three CLK edges later, the command outputs will go active (see timing waveforms). The Multibus requires this delay for the address and data to be valid on the bus before the commands become active.

When MB = 0, CEN/$\overline{\text{AEN}}$ becomes CEN. CEN is an asynchronous input which immediately affects the command and DEN outputs. When CEN makes a high-to-low transition, the commands and DEN are immediately forced inactive. When CEN makes a low-to-high transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{\text{READY}}$ must still become active to terminate a bus cycle if CEN remains low for a selected bus controller (CENL was latched high).

Some memory or I/O systems may require more address or write data setup time to command active than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled low to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/$\overline{\text{R}}$.

CMDLY is first sampled on the falling edge of the CLK ending TS. If sampled high, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled low, the proper command output becomes active immediately if MB = 0. If MB = 1, the proper command goes active no earlier than shown in the figures on pages 12 and 13.

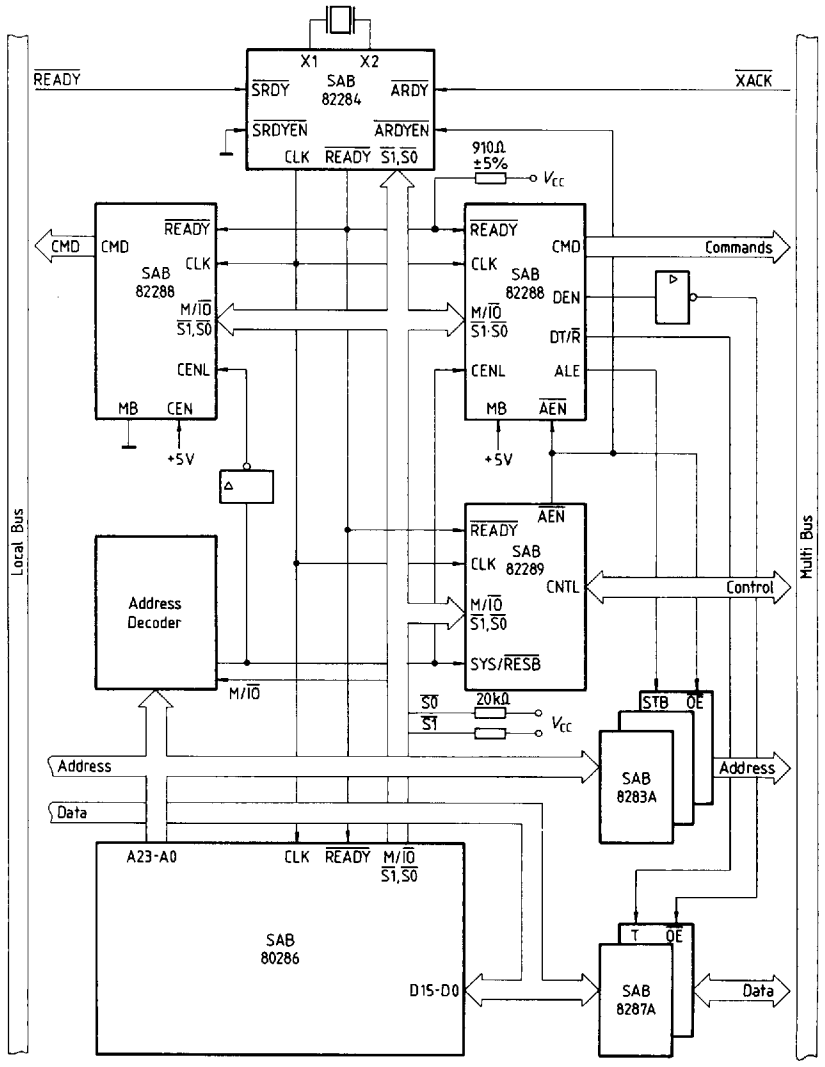
$\overline{\text{READY}}$ can terminate a bus cycle before CMDLY allows a command to be issued. In this case no commands are issued and the bus controller will deactivate DEN and DT/$\overline{\text{R}}$ in the same manner as if a command had been issued.

Waveforms

The waveforms show the timing relationships of inputs and outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed. The waveforms provide some functional descriptions of the SAB 82288; however, most functional descriptions are provided in the figures of section Functional Description.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

System Use of $\overline{AEN}$ and CENL



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Absolute Maximum Ratings

Ambient temperature under bias . . . . . 0 to 70°C
Storage temperature . . . . . −65 to +150°C
Voltage on any pin with respect to GND . . . . . −0.5 to +7V
Power dissipation . . . . . 1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ±10%

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Power supply current	I_{CC}	–	100	mA	–
Forward input current ($\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$)	I_F	–	−0.5	mA	V_F = 0.45 V
Input leakage current (all other)	I_{LI}	–	±10	µA	0 V ≦ V_{IN} ≦ V_{CC}
Output leakage current	I_{LO}	–	±10	µA	0.45 V ≦ V_{OUT} ≦ V_{CC}
Low output voltage Command outputs Control outputs	V_{OL}	–	0.45	V	I_{OL} = 32 mA I_{OL} = 16 mA
High output voltage Command outputs Control outputs	V_{OH}	2.4	–	V	I_{OH} = −5 mA I_{OH} = −1 mA
Low input voltage	V_{IL}	−0.5	0.8	V	–
CLK low input voltage	V_{CL}	−0.5	0.6	V	–
High input voltage	V_{IH}	2.0	V_{CC} +0.5	V	–
CLK high input voltage	V_{CH}	3.8		V	–

Capacitance

T_A = 25°C, V_{CC} = GND = 0 V, f_C = 1 MHz

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
CLK input capacitance	C_{CLK}	–	12	pF	Unmeasured pins returned to GND
Input capacitance	C_I	–	10	pF	
Input/output capacitance	C_{IO}	–	20	pF	

Note: Not 100%, guaranteed by design characterization.

AC Characteristics SAB 82288

Unless otherwise specified, the AC timings are referred to signal points of 0.8 V and 2.0 V as illustrated in the waveforms.

T_A = 0 to 70°C, V_{CC} = 5V ±10%

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
CLK period	t_1	62	250	ns	–
CLK high time	t_2	20	235	ns	at 3.6 V
CLK low time	t_3	15	230	ns	at 1.0 V
CLK rise time	t_4	–	10	ns	1.0 to 3.6 V
CLK fall time	t_5	–	10	ns	3.6 to 1.0 V
M/$\overline{IO}$ and status setup time	t_6	22	–	ns	–
M/$\overline{IO}$ and status hold time	t_7	0	–	ns	–
CENL setup time	t_8	20	–	ns	–
CENL hold time	t_9	0	–	ns	–
$\overline{READY}$ setup time	t_{10}	38	–	ns	–
$\overline{READY}$ hold time	t_{11}	25	–	ns	–
CMDLY setup time	t_{12}	20	–	ns	–
CMDLY hold time	t_{13}	0	–	ns	–
$\overline{AEN}$ setup time	t_{14}	20	–	ns	1)
$\overline{AEN}$ hold time	t_{15}	0	–	ns	1)
ALE, MCE active delay	t_{16}	3	20	ns	2)
ALE, MCE inactive delay	t_{17}	–	20	ns	2)
DEN (write) inactive from CENL	t_{18}	–	35	ns	2)
DT/$\overline{R}$ low from CLK	t_{19}	–	25	ns	2)
DEN (read) active from DT/$\overline{R}$	t_{20}	5	35	ns	2)
DEN (read) inactive delay	t_{21}	3	35	ns	2)
DT/$\overline{R}$ high from DEN inactive	t_{22}	5	35	ns	2)
DEN (write) active delay	t_{23}	–	30	ns	2)
DEN (write) inactive delay	t_{24}	3	30	ns	2)
DEN inactive from CEN	t_{25}	–	25	ns	2)
DEN active from CEN	t_{26}	–	30	ns	2)
DT/$\overline{R}$ high from CLK and CEN	t_{27}	–	35	ns	2) 3)

Notes see next page

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AC Characteristics SAB 82288 (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
DEN active from $\overline{AEN}$	t_{28}	–	30	ns	[2]
Command active delay	t_{29}	3	25	ns	[4]
Command inactive delay	t_{30}	3	25	ns	[4]
Command inactive from CEN	t_{31}	–	25	ns	[4]
Command active from CEN	t_{32}	–	25	ns	[4]
Command valid delay from $\overline{AEN}$	t_{33}	–	40	ns	[4]
Command float time	t_{34}	–	40	ns	[4]
MB setup time	t_{35}	20	–	ns	–
MB hold time	t_{36}	0	–	ns	–
Command inactive enable from MB↓	t_{37}	–	40	ns	[4]
Command float time from MB↑	t_{38}	–	40	ns	–
DEN inactive from MB↑	t_{39}	–	30	ns	[2]
DEN active from MB↓	t_{40}	–	35	ns	[2]

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

[2] Control output load: $C_L = 150$ pF, $I_{OL} = 16$ mA, $I_{OH} = -1$ mA.

[3] t_{27} only applies to bus cycles where MB = 0, the SAB 82288 was selected, and DEN = 0 when the cycle is terminated (because CEN = 0).

[4] Command output load: $C_L = 300$ pF, $I_{OL} = 32$ mA, $I_{OH} = -5$ mA.

AC Characteristics SAB 82288-6

Unless otherwise specified, the AC timings are referred to signal points of 0.8 V and 2.0 V as illustrated in the waveforms.

$T_A = 0$ to 70°C, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
CLK period	t_1	83	250	ns	–
CLK high time	t_2	25	235	ns	at 3.6 V
CLK low time	t_3	20	225	ns	at 1.0 V
CLK rise time	t_4	–	10	ns	1.0 to 3.6 V
CLK fall time	t_5	–	10	ns	3.6 to 1.0 V
M/$\overline{IO}$ and status setup time	t_6	28	–	ns	–
M/$\overline{IO}$ and status hold time	t_7	0	–	ns	–
CENL setup time	t_8	30	–	ns	–
CENL hold time	t_9	0	–	ns	–
$\overline{READY}$ setup time	t_{10}	50	–	ns	–
$\overline{READY}$ hold time	t_{11}	35	–	ns	–
CMDLY setup time	t_{12}	25	–	ns	–
CMDLY hold time	t_{13}	0	–	ns	–
$\overline{AEN}$ setup time	t_{14}	25	–	ns	1)
$\overline{AEN}$ hold time	t_{15}	0	–	ns	1)
ALE, MCE active delay	t_{16}	3	25	ns	2)
ALE, MCE inactive delay	t_{17}	–	35	ns	2)
DEN (write) inactive from CENL	t_{18}	–	35	ns	2)
DT/$\overline{R}$ low from CLK	t_{19}	–	40	ns	2)
DEN (read) active from DT/$\overline{R}$	t_{20}	5	50	ns	2)
DEN (read) inactive delay	t_{21}	3	40	ns	2)
DT/$\overline{R}$ high from DEN inactive	t_{22}	5	45	ns	2)
DEN (write) active delay	t_{23}	–	35	ns	2)
DEN (write) inactive delay	t_{24}	3	35	ns	2)
DEN inactive from CEN	t_{25}	–	40	ns	2)
DEN active from CEN	t_{26}	–	35	ns	2)
DT/$\overline{R}$ high from CLK and CEN	t_{27}	–	50	ns	2) 3)

Notes see next page

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AC Characteristics SAB 82288-6 (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
DEN active from $\overline{AEN}$	t_{28}	–	35	ns	[2]
Command active delay	t_{29}	3	40	ns	[4]
Command inactive delay	t_{30}	3	30	ns	[4]
Command inactive from CEN	t_{31}	–	35	ns	[4]
Command active from CEN	t_{32}	–	45	ns	[4]
Command valid delay from $\overline{AEN}$	t_{33}	–	40	ns	[4]
Command float time	t_{34}	–	40	ns	[4]
MB setup time	t_{35}	25	–	ns	–
MB hold time	t_{36}	0	–	ns	–
Command inactive enable from MB↓	t_{37}	–	40	ns	[4]
Command float time from MB↑	t_{38}	–	40	ns	–
DEN inactive from MB↑	t_{39}	–	40	ns	[2]
DEN active from MB↓	t_{40}	–	35	ns	[2]

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

[2] Control output load: $C_L = 150$ pF, $I_{OL} = 16$ mA, $I_{OH} = -1$ mA.

[3] t_{27} only applies to bus cycles where MB = 0, the SAB 82288 was selected, and DEN = 0 when the cycle is terminated (because CEN = 0).

[4] Command output load: $C_L = 300$ pF, $I_{OL} = 32$ mA, $I_{OH} = -5$ mA.

AC Characteristics SAB 82288-1

Unless otherwise specified, the AC timings are referred to signal points of 0.8 V and 2.0 V as illustrated in the waveforms.

T_A = 0 to 70°C, V_{CC} = 5 V ±10%

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
CLK period	t_1	50	250	ns	–
CLK high time	t_2	16	235	ns	at 3.6 V
CLK low time	t_3	12	230	ns	at 1.0 V
CLK rise time	t_4	–	8	ns	1.0 to 3.6 V
CLK fall time	t_5	–	8	ns	3.6 to 1.0 V
M/$\overline{IO}$ and status setup time	t_6	18	–	ns	–
M/$\overline{IO}$ and status hold time	t_7	0	–	ns	–
CENL setup time	t_8	15	–	ns	–
CENL hold time	t_9	0	–	ns	–
$\overline{READY}$ setup time	t_{10}	26	–	ns	–
$\overline{READY}$ hold time	t_{11}	25	–	ns	–
CMDLY setup time	t_{12}	15	–	ns	–
CMDLY hold time	t_{13}	0	–	ns	–
$\overline{AEN}$ setup time	t_{14}	15	–	ns	1)
$\overline{AEN}$ hold time	t_{15}	0	–	ns	1)
ALE, MCE active delay	t_{16}	3	16	ns	2)
ALE, MCE inactive delay	t_{17}	–	19	ns	2)
DEN (write) inactive from CENL	t_{18}	–	23	ns	2)
DT/$\overline{R}$ low from CLK	t_{19}	–	23	ns	2)
DEN (read) active from DT/$\overline{R}$	t_{20}	5	21	ns	2)
DEN (read) inactive delay	t_{21}	3	21	ns	2)
DT/$\overline{R}$ high from DEN inactive	t_{22}	5	20	ns	2)
DEN (write) active delay	t_{23}	–	23	ns	2)
DEN (write) inactive delay	t_{24}	3	19	ns	2)
DEN inactive from CEN	t_{25}	–	25	ns	2)
DEN active from CEN	t_{26}	–	24	ns	2)
DT/$\overline{R}$ high from CLK and CEN	t_{27}	–	25	ns	2) 3)

Notes see next page

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AC Characteristics SAB 82288-1 (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
DEN active from $\overline{AEN}$	t_{28}	–	26	ns	[2]
Command active delay	t_{29}	3	21	ns	[4]
Command inactive delay	t_{30}	3	20	ns	[4]
Command inactive from CEN	t_{31}	–	25	ns	[4]
Command active from CEN	t_{32}	–	25	ns	[4]
Command valid delay from $\overline{AEN}$	t_{33}	–	40	ns	[4]
Command float time	t_{34}	–	40	ns	[4]
MB setup time	t_{35}	20	–	ns	–
MB hold time	t_{36}	0	–	ns	–
Command inactive enable from MB↓	t_{37}	–	40	ns	[4]
Command float time from MB↑	t_{38}	–	40	ns	–
DEN inactive from MB↑	t_{39}	–	26	ns	[2]
DEN active from MB↓	t_{40}	–	35	ns	[2]

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

[2] Control output load: $C_L = 150$ pF, $I_{OL} = 16$ mA, $I_{OH} = -1$ mA.

[3] t_{27} only applies to bus cycles where MB = 0, the SAB 82288 was selected, and DEN = 0 when the cycle is terminated (because CEN = 0).

[4] Command output load: $C_L = 300$ pF, $I_{OL} = 32$ mA, $I_{OH} = -5$ mA.

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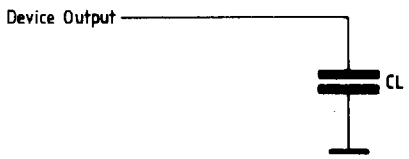
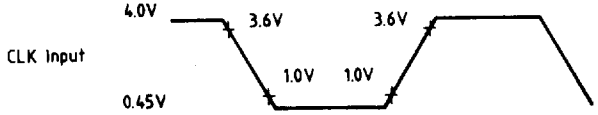
AC Testing Waveforms

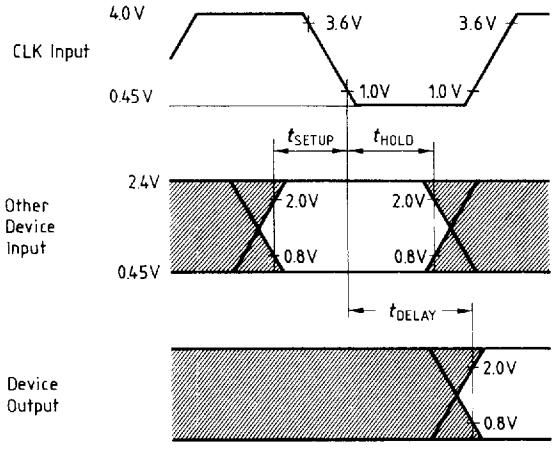
Test Loading on Outputs



Drive and Measurement Points – CLK Input



Setup, Hold and Delay Time Measurement – General



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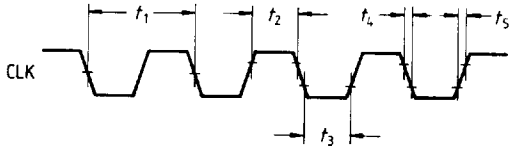
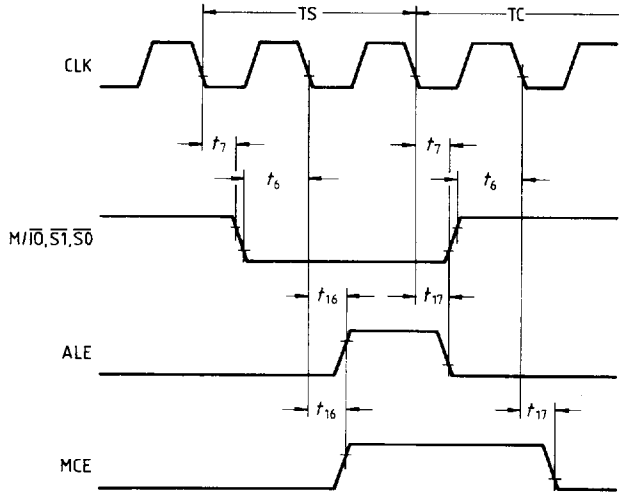
Waveforms

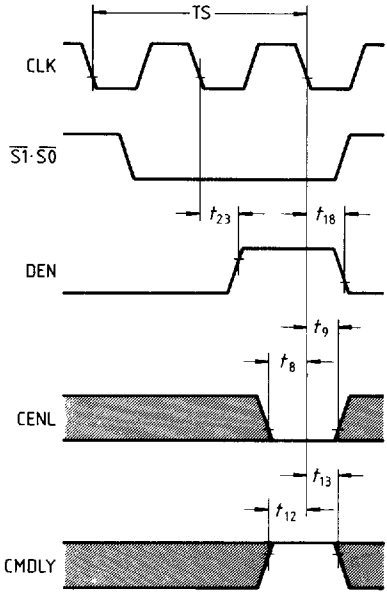
CLK Characteristics



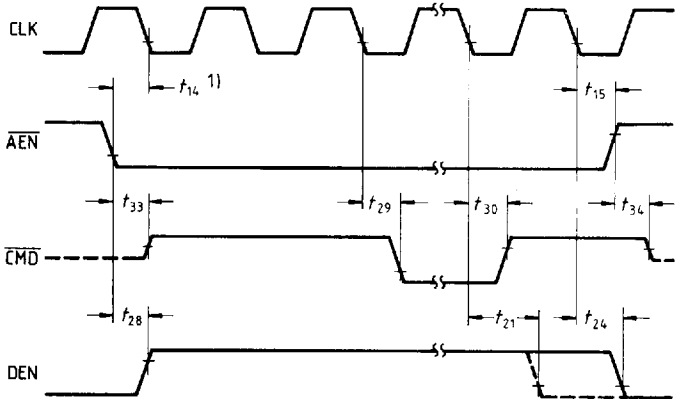
Status, ALE, MCE Characteristics



CENL, CMDLY, DEN Characteristics with MB = 0 and CEN = 1 during Write Cycle



AEN Characteristics with MB = 1



1) AEN is an asynchronous input. AEN setup and hold time is specified to guarantee the response shown in the waveforms.

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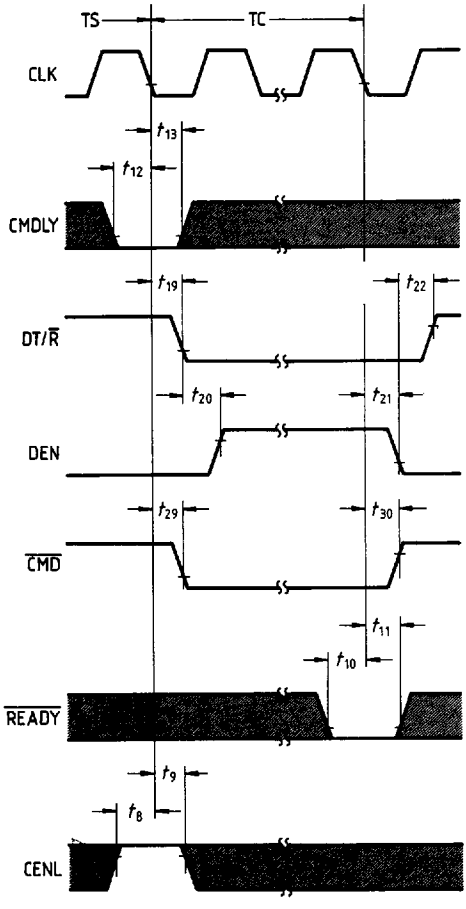
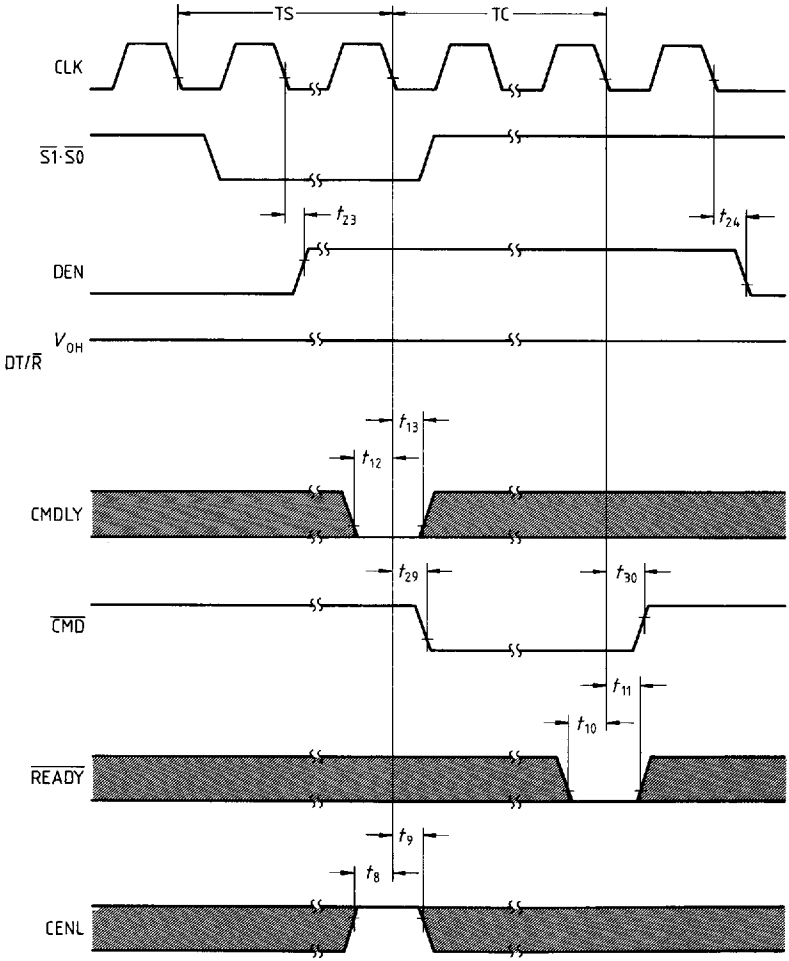
Read Cycle Characteristics with MB = 0 and CEN = 1



Write Cycle Characteristics with MB = 0 and CEN = 1



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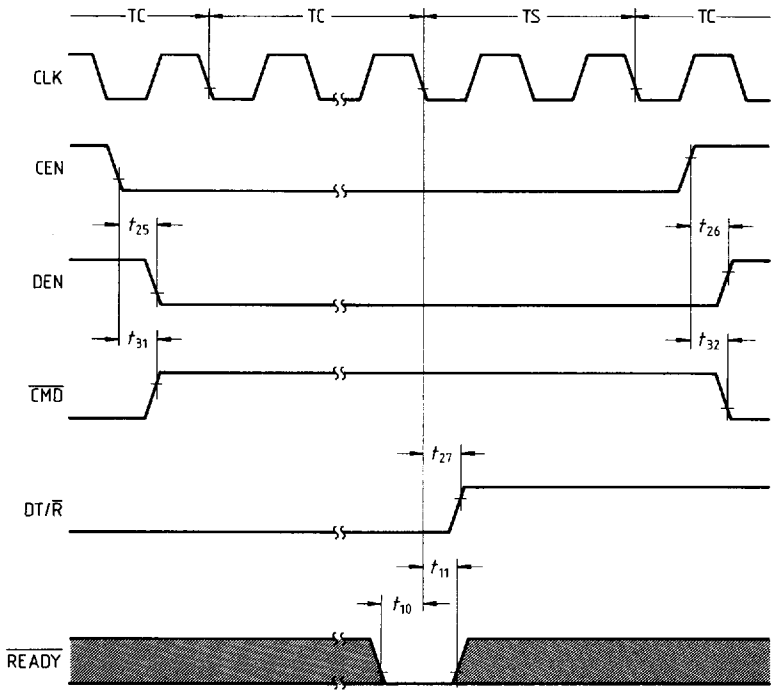
CEN Characteristics with MB = 0



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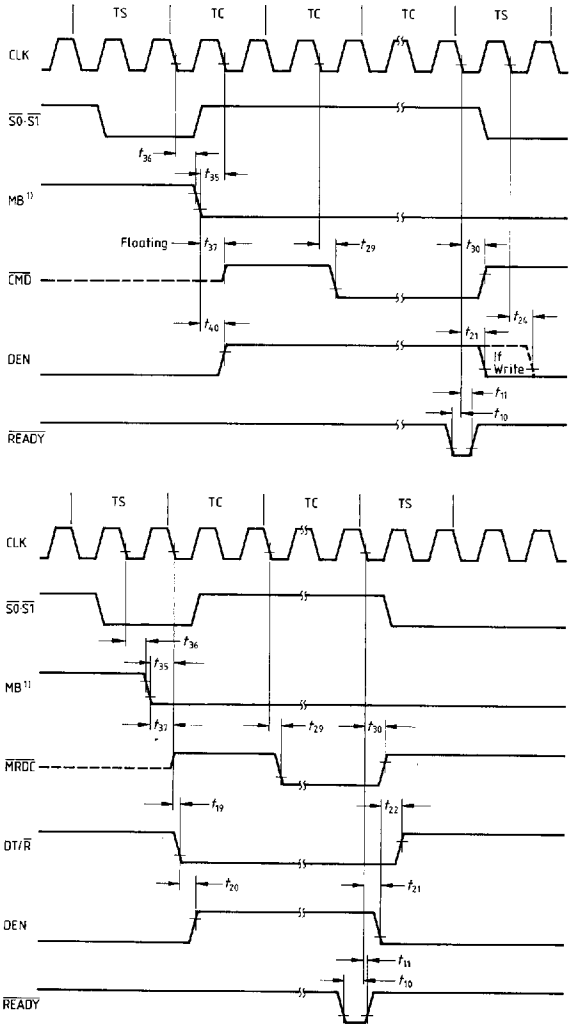
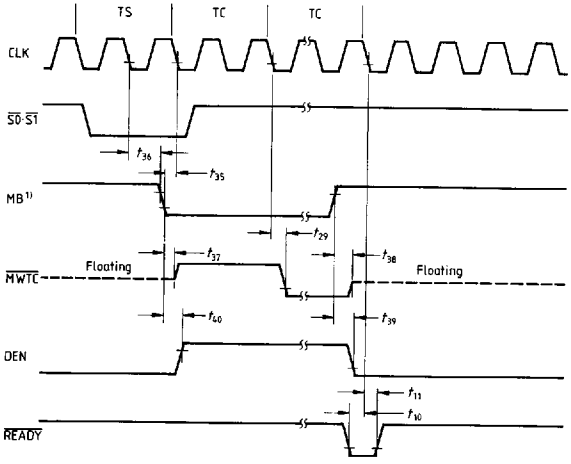
MB Characteristics with $\overline{AEN}$/CEN = High



1) MB is an asynchronous input. MB setup and hold times specified to guarantee the response shown in the waveforms.

If the setup time t_{35} is met, two clock cycles will occur before $\overline{CMD}$ becomes active after the falling edge of MB.

MB Characteristics with $\overline{AEN}$/CEN = High (cont'd)



1) MB is an asynchronous input. MB setup and hold times specified to guarantee the response shown in the waveforms.

If the setup time t_{35} is met, two clock cycles will occur before $\overline{CMD}$ becomes active after the falling edge of MB.