# MSX2 Prototype board revisions.

Application: S-100 UTILITY VERSION 01



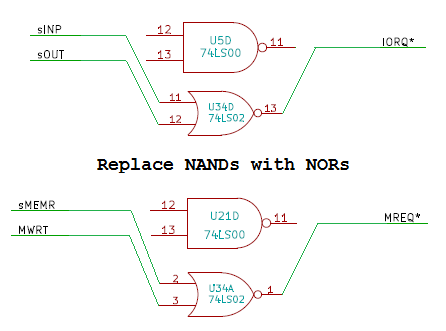
**Revision 1** – Replace the NAND gates used to generate IORQ\* and MREQ\* with NORs.

**Revision 2** – Correct the circuit used to enable the on board EPROM before the PPI control pins are initialized.

2/2/2012 – Neil Breeden – Initial creation of this document.

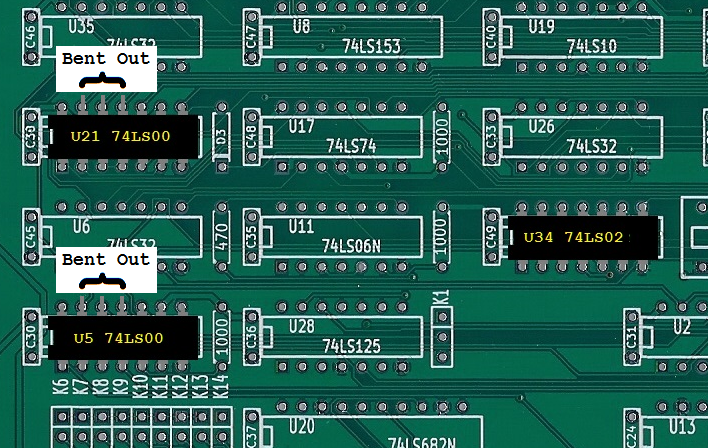
## Revision 1:

IORQ\* and MREQ\* are not being generated. The NAND gates (U5D and U21D) will be replaced with NOR gates. There are two spares (U34A and U34D) that can be used.



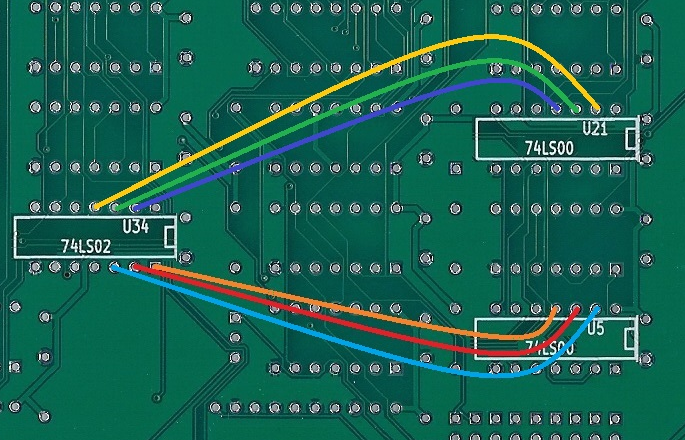
## Revision 1 continued:

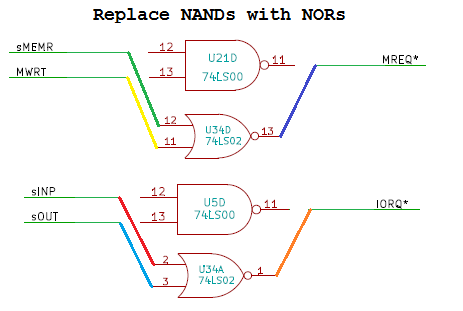
I did this by bending out pins 11, 12 and 13 of U5 and U21. The three chips involved in the fix are shown below. These pins may be bent out and left floating; as this is LS TTL logic leaving the input pins floating will result in them pulling themselves high. Make sure that these pins do not touch any pins on U6 and U35.



## Revision 1 continued:

Jumper wires are then used on the back of the board to connect to the NOR games. Note that the silk screens on the image below were added to the image and do not exist on the actual board.





## Revision 2 – Power on reset fix.

On power up or RESET the on board EPROM is not available to the CPU; this is due to how the MSX2 controls SLOTS. The system however needs to access to EPROM at power up so that the code to initialize the PPI can be ran which enables the slot controls. This is a chicken before the egg issue.

A set/reset flip flop is used to manage this situation. On power or reset the flip flop enables the EPROM to be available without the PPI being initialized. Once the PPI has been initialized the Y5 signal (used to scan the MSX2 keyboard) toggles the flip flop allowing the slot controls to work.

You can reference the Goldstar MSX2 design for additional details.

## 

## Revision 2 Continued:

U21 Pin 1 is bent out. A 470pF disc cap is connected from it to VSS (GND). U21 Pin1 is then connected to U12 Pin 6.

## 

## 

