

*Totally Logical*

DATA SHEET

## Z8S180/Z8L180

ENHANCED Z180 MICROPROCESSOR OFFERS  
FASTER EXECUTION,  
POWER-SAVER MODE, LOW EMI

### FEATURES

- Code Compatible with ZiLOG Z80<sup>®</sup> CPU
- Extended Instructions
- Two Chain-Linked DMA Channels
- Low Power-Down Modes
- On-Chip Interrupt Controllers
- Three On-Chip Wait-State Generators
- On-Chip Oscillator/Generator
- Expanded MMU Addressing (Up to 1 MB)
- Clocked Serial I/O Port
- Two 16-Bit Counter/Timers
- Two Enhanced UARTs (up to 512 Kbps)
- Clock Speeds: 10, 20, 33 MHz
- Operating Range: 5V (3.3V@ 20 MHz)
- Operating Temperature Range: 0°C to +70°C
- -40°C to +85°C Extended Temperature Range
- Three Packaging Styles
  - 68-Pin PLCC
  - 64-Pin DIP
  - 80-Pin QFP

### GENERAL DESCRIPTION

The enhanced Z8S180/Z8L180<sup>™</sup> significantly improves on the previous Z80180 models while still providing full backward compatibility with existing ZiLOG Z80 devices. The Z8S180/Z8L180 now offers faster execution speeds, power-saving modes, and EMI noise reduction.

This enhanced Z180<sup>™</sup> design also incorporates additional feature enhancements to the ASCIs, DMAs, and I<sub>CC</sub> STANDBY mode power consumption. With the addition of ESCC-like Baud Rate Generators (BRGs), the two ASCIs now have the flexibility and capability to transfer data asynchronously at rates of up to 512 Kbps. In addition, the ASCII receiver has added a 4-byte first in/first out (FIFO) buffer which can be used to store incoming data to reduce the incidence of overrun errors. The DMAs have been modified to allow for a chain-linking of the two DMA channels when set to take their DMA requests from the same peripherals device. This feature allows for nonstop DMA operation between the two DMA channels, reducing the amount of CPU intervention (Figure 1).

Not only does the Z8S180/Z8L180 consume less power during normal operations than the previous model, it has

also been designed with three modes intended to further reduce the power consumption. ZiLOG reduced I<sub>CC</sub> power consumption during STANDBY Mode to a minimum of 10  $\mu$ A by stopping the external oscillators and internal clock. The SLEEP mode reduces power by placing the CPU into a stopped state, consuming less current while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a stopped mode, reducing power consumption even further.

A new clock-doubler feature has been implemented into the Z8S180/Z8L180 device that allows the programmer to double the internal clock speed from that of the external clock. This provides a system cost savings by allowing the use of lower-cost, lower-frequency crystals instead of higher-cost, higher-speed oscillators.

The Enhanced Z180 is housed in 80-pin QFP, 68-pin PLCC, and 64-pin DIP packages.

**Note:** All Signals with an overline,  $\overline{\hspace{0.5cm}}$ , are active Low.  
For example: B/W, in which WORD is active Low;  
or B/W, in which BYTE is active Low.

Power connections follow the conventional descriptions below:

Connection	Circuit	Device
Power	$V_{CC}$	$V_{DD}$
Ground	GND	$V_{SS}$

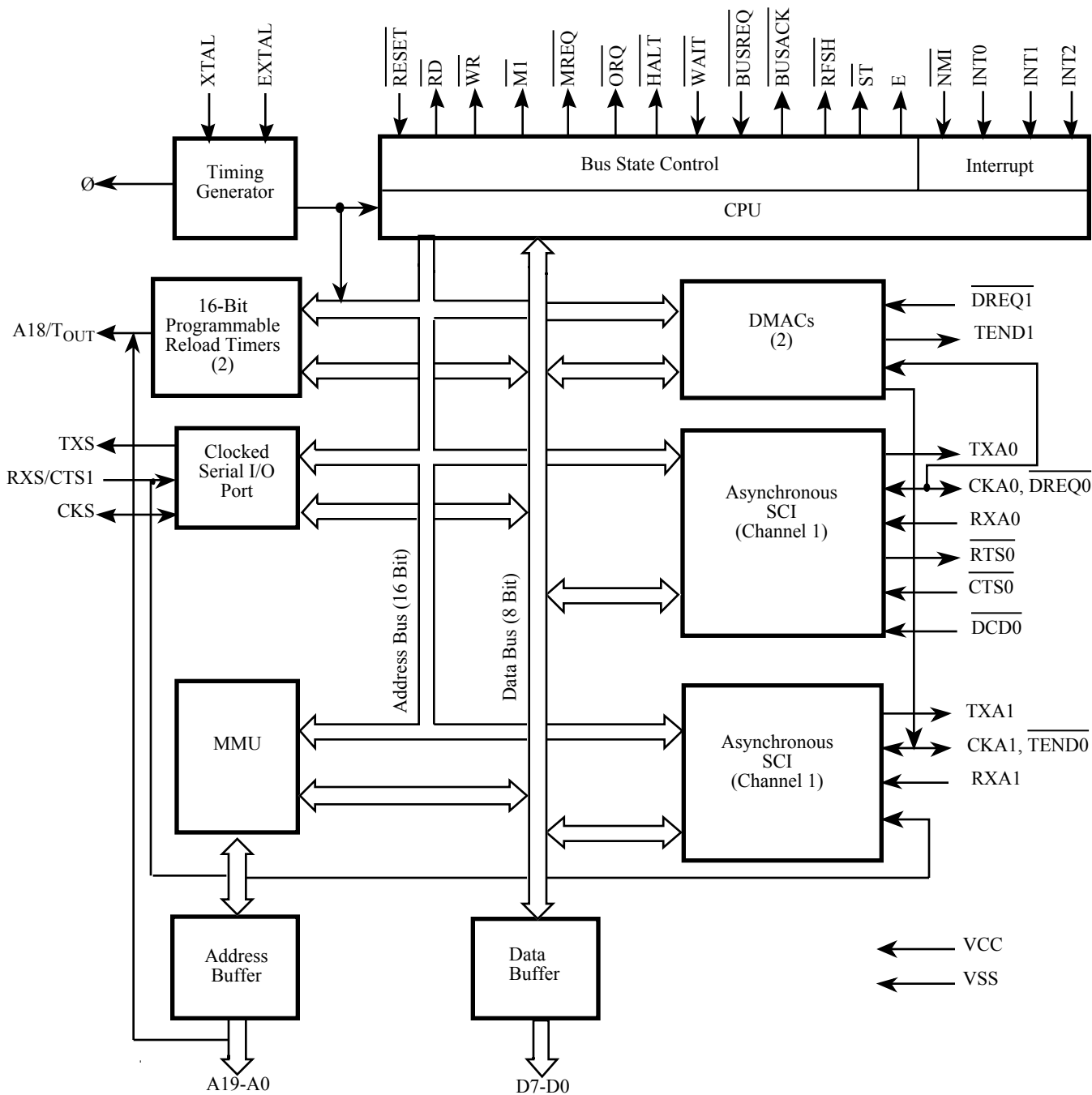


Figure 1. Z8S180/Z8L180 Functional Block Diagram

PIN IDENTIFICATION

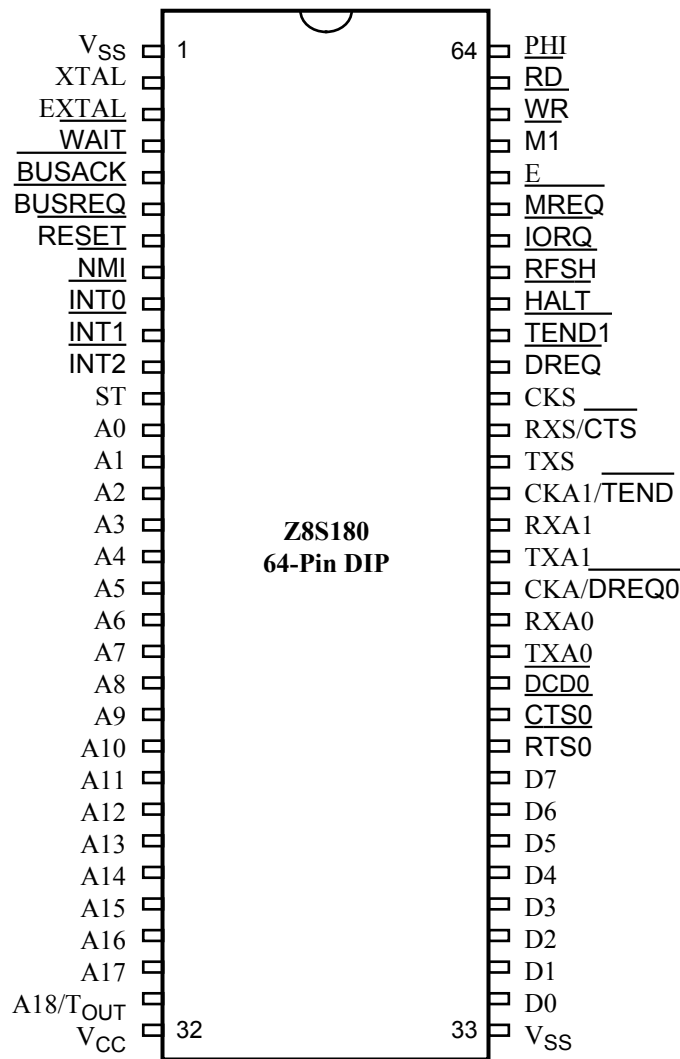


Figure 2. Z8S180 64-Pin DIP Pin Configuration

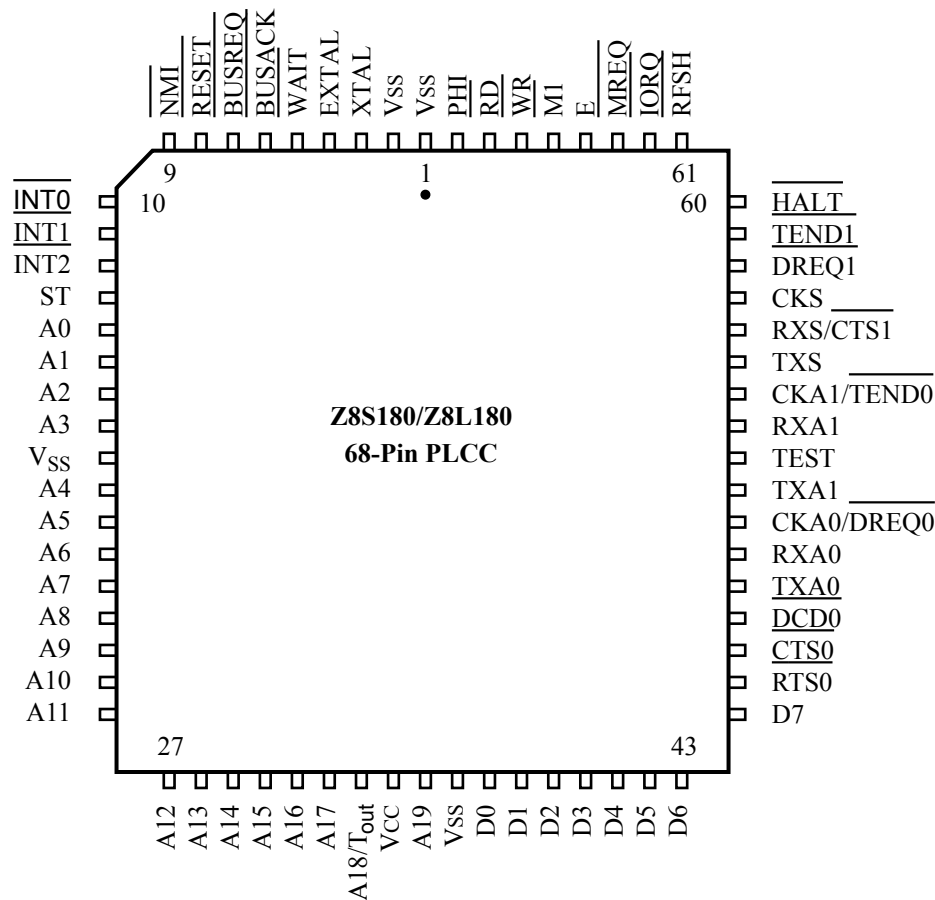


Figure 3. Z8S180/Z8L180 68-Pin PLCC Pin Configuration

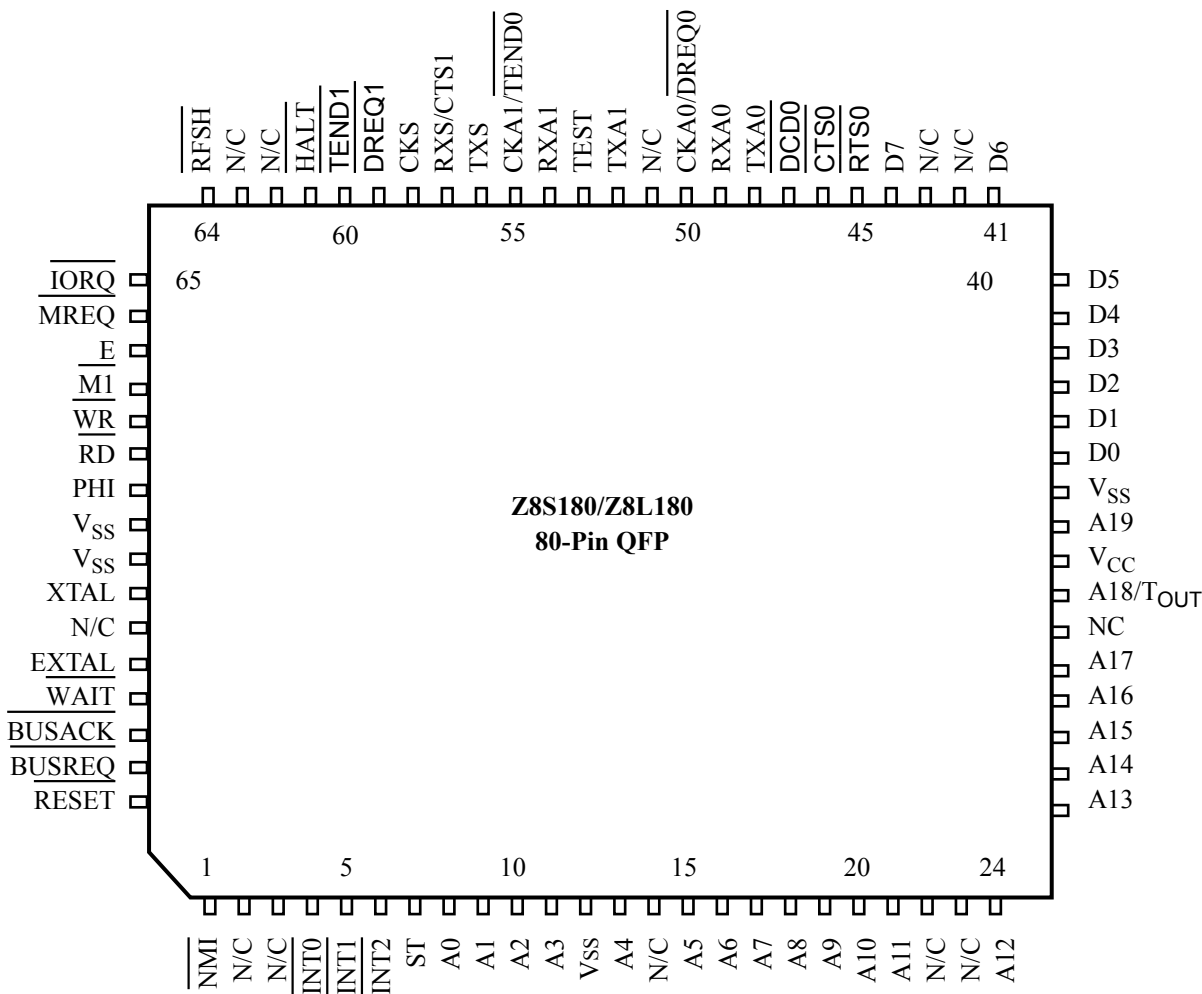


Figure 4. Z8S180/Z8L180 80-Pin QFP Pin Configuration

**PIN IDENTIFICATION** (Continued)

*Table 1. Z8S180/Z8L180 Pin Identification*

Pin Number and Package Type			Secondary		
QFP	PLCC	DIP	Default Function	Function	Control
1	9	8	NMI		
2			NC		
3			NC		
4	10	9	INT0		
5	11	10	INT1		
6	12	11	INT2		
7	13	12	ST		
8	14	13	A0		
9	15	14	A1		
10	16	15	A2		
11	17	16	A3		
12	18		V <sub>SS</sub>		
13	19	17	A4		
14			NC		
15	20	18	A5		
16	21	19	A6		
17	22	20	A7		
18	23	21	A8		
19	24	22	A9		
20	25	23	A10		
21	26	24	A11		
22			NC		
23			NC		
24	27	25	A12		
25	28	26	A13		
26	29	27	A14		
27	30	28	A15		
28	31	29	A16		
29	32	30	A17		
30			NC		
31	33	31	A18	$\overline{T}_{OUT}$	Bit 2 or Bit 3 of TCR
32	34	32	V <sub>CC</sub>		
33	35		A19		

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Pin Number and Package Type			Default Function	Secondary Function	Control
QFP	PLCC	DIP			
34	36	33	V <sub>SS</sub>		
35	37	34	D0		
36	38	35	D1		
37	39	36	D2		
38	40	37	D3		
39	41	38	D4		
40	42	39	D5		
41	43	40	D6		
42			NC		
43			NC		
44	44	41	D7		
45	45	42	<u>RTS0</u>		
46	46	43	<u>CTS0</u>		
47	47	44	DCD0		
48	48	45	TXA0		
49	49	46	RXA0		
50	50	47	CKA0	<u>DREQ0</u>	Bit 3 or Bit 5 of DMODE
51			NC		
52	51	48	TXA1		
53	52		TEST		
54	53	49	RXA1		
55	54	50	CKA1	<u>TEND0</u>	Bit 4 of CNTLA1
56	55	51	TXS		
57	56	52	RXS	<u>CTS1</u>	Bit 2 of STAT1
58	57	53	<u>CKS</u>		
59	58	54	<u>DREQ1</u>		
60	59	55	<u>TEND1</u>		
61	60	56	<u>HALT</u>		
62			NC		
63			NC		
64	61	57	<u>RFSH</u>		
65	62	58	<u>IORQ</u>		
66	63	59	<u>MREQ</u>		
67	64	60	E		
68	65	61	<u>M1</u>		
69	66	62	<u>WR</u>		

*Table 1. Z8S180/Z8L180 Pin Identification (Continued)*

Pin Number and Package Type			Secondary	Control
QFP	PLCC	DIP	Default Function	Function
70	67	63	RD	
71	68	64	PHI	
72	1	1	V <sub>SS</sub>	
73	2		V <sub>SS</sub>	
74	3	2	XTAL	
75			NC	
76	4	3	EXTAL	
77	5	4	WAIT	
78	6	5	BUSACK	
79	7	6	BUSREQ	
80	8	7	RESET	

*Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes*

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
1	9	8	NMI		IN	IN	IN
2			NC				
3			NC				
4	10	9	INT0		IN	IN	IN
5	11	10	INT1		IN	IN	IN
6	12	11	INT2		IN	IN	IN
7	13	12	ST		1	?	1
8	14	13	A0		3T	3T	1
9	15	14	A1		3T	3T	1
10	16	15	A2		3T	3T	1
11	17	16	A3		3T	3T	1
12	18		V <sub>SS</sub>		GND	GND	GND
13	19	17	A4		3T	3T	1
14			NC				
15	20	18	A5		3T	3T	1
16	21	19	A6		3T	3T	1
17	22	20	A7		3T	3T	1
18	23	21	A8		3T	3T	1
19	24	22	A9		3T	3T	1



Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
20	25	23	A10		3T	3T	1
21	26	24	A11		3T	3T	1
22			NC				
23			NC				
24	27	25	A12		3T	3T	1
25	28	26	A13		3T	3T	1
26	29	27	A14		3T	3T	1
27	30	28	A15		3T	3T	1
28	31	29	A16		3T	3T	1
29	32	30	A17		3T	3T	1
30			NC				
31	33	31	A18	T <sub>OUT</sub>	3T	3T	1
32	34	32	V <sub>CC</sub>		V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
33	35		A19		3T	3T	1
34	36	33	V <sub>SS</sub>		GND	GND	GND
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	RTS0		1	OUT	1
46	46	43	CTS0		IN	OUT	IN
47	47	44	DCD0		IN	IN	IN
48	48	45	TXA0		1	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0	DREQ0	3T	OUT	OUT
51			NC				
52	51	48	TXA1		1	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN

*Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes*

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
55	54	50	CKA1	TEND0	3T	IN	IN
56	55	51	TXS		1	OUT	OUT
57	56	52	RXS	CTS1	IN	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	DREQ1		IN	3T	IN
60	59	55	TEND1		1	OUT	1
61	60	56	HALT		1	1	0
62			NC				
63			NC				
64	61	57	RFSH		1	OUT	OUT
65	62	58	IORQ		1	3T	1
66	63	59	MREQ		1	3T	1
67	64	60	E		0	OUT	OUT
68	65	61	M1		1	1	1
69	66	62	WR		1	3T	1
70	67	63	RD		1	3T	1
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V <sub>SS</sub>		GND	GND	GND
73	2		V <sub>SS</sub>		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				
76	4	3	EXTAL		IN	IN	IN
77	5	4	WAIT		IN	IN	IN
78	6	5	BUSACK		1	OUT	OUT
79	7	6	BUSREQ		IN	IN	IN
80	8	7	RESET		IN	IN	IN

## PIN DESCRIPTIONS

**A0–A19.** Address Bus (Output, active High, tri-state). A<sub>0</sub>–A<sub>19</sub> form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 1 MB) and I/O data bus exchanges (up to 64K). The address bus enters a high-impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (T<sub>OUT</sub>, selected as address output on reset), and address line A19 is not available in DIP versions of the Z8S180.

**BUSACK.** Bus Acknowledge (Output, active Low). BUSACK indicates that the requesting device, the MPU address and data bus, and some control signals have entered their high-impedance state.

**BUSREQ.** Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than NMI and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions, places addresses, data buses, and other control signals into the high-impedance state.

**CKA0, CKA1.** Asynchronous Clock 0 and 1 (Bidirectional, active High). When in output mode, these pins are the transmit and receive clock outputs from the ASCII baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCII baud rate generators. CKA0 is multiplexed with DREQ0, and CKA1 is multiplexed with TEND0.

**CKS.** Serial Clock (Bidirectional, active High). This line is the clock for the CSIO channel.

**PHI CLOCK.** System Clock (Output, active High). The output is used as a reference clock for the MPU and the external system. The frequency of this output is equal to one-half that of the crystal or input clock frequency.

**CTS0–CTS1.** Clear to send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCII channels. CTS1 is multiplexed with RXS.

**D0–D7.** Data Bus = (Bidirectional, active High, tri-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

**DCD0.** Data Carrier Detect 0 (Input, active Low). This is a programmable modem control signal for ASCII channel 0.

**DREQ0, DREQ1.** DMA Request 0 and 1 (Input, active Low). DREQ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a read or write operation. These inputs can be

programmed to be either level or edge sensed. DREQ0 is multiplexed with CKA0.

**E.** Enable Clock (Output, active High). This pin functions as a synchronous, machine-cycle clock output during bus transactions.

**EXTAL.** External Clock Crystal (Input, active High). Crystal oscillator connections. An external clock can be input to the Z8S180/Z8L180 on this pin when a crystal is not used. This input is Schmitt triggered.

**HALT.** HALT/SLEEP (Output, active Low). This output is asserted after the CPU has executed either the HALT or SLEEP instruction and is waiting for either a nonmaskable or a maskable interrupt before operation can resume. It is also used with the M1 and ST signals to decode the status of the CPU machine cycle.

**INT0.** Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the NMI and BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the M1 and IORQ signals become active.

**INT1, INT2.** Maskable Interrupt Request 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the NMI, BUSREQ, and INT0 signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for INT0, neither the M1 or IORQ signals become active during this cycle.

**IORQ.** I/O Request (Output, active Low, tri-state). IORQ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. IORQ is also generated, along with M1, during the acknowledgment of the INT0 input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the IOE signal of the Z64180.

**M1.** Machine Cycle 1 (Output, active Low). Together with MREQ, M1 indicates that the current cycle is the opcode-fetch cycle of instruction execution. Together with IORQ, M1 indicates that the current cycle is for interrupt acknowledgment. It is also used with the HALT and ST signal to decode the status of the CPU machine cycle. This signal is analogous to the LIR signal of the Z64180.

**MREQ.** Memory Request (Output, active Low, tri-state). MREQ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the ME signal of Z64180.

**NMI.** Nonmaskable Interrupt (Input, negative edge triggered). NMI has a higher priority than INT and is always

recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

**RD.** ReOp-coded (Output, active Low, tri-state).  $\overline{\text{RD}}$  indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

**RFSH.** Refresh (Output, active Low). Together with MREQ, RFSH indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A10) contain the refresh address. *This signal is analogous to the REF signal of the Z64180.*

**RTS0.** Request to Send 0 (Output, active Low). This is a programmable MODEM control signal for ASCII channel 0.

**RXA0, RXA1.** Receive Data 0 and 1 (Input, active High). These signals are the receive data for the ASCII channels.

**RXS.** Clocked Serial Receive Data (Input, active High). This line is the receive data for the CSIO channel. RXS is multiplexed with the CTS1 signal for ASCII channel 1.

**ST.** Status (Output, active High). This signal is used with the M1 and HALT output to decode the status of the CPU machine cycle.

**Table 3. Status Summary**

ST	HALT	M1	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)

Notes:

X = Reserved

MC = Machine Cycle

**TEND0, TEND1.** Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent write cycle of a DMA operation. It is used to indicate the end of the block transfer. TEND0 is multiplexed with CKA1.

**TEST.** Test (Output, not in DIP version). This pin is for test and should be left open.

**TOUT.** Timer Out (Output, active High). T<sub>OUT</sub> is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus.

**TXA0, TXA1.** Transmit Data 0 and 1 (Outputs, active High). These signals are the transmitted data from the ASCII channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

**TXS.** Clocked Serial Transmit Data (Output, active High). This line is the transmitted data from the CSIO channel.

**WAIT.** Wait (Input, active Low).  $\overline{\text{WAIT}}$  indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the WAIT input is sampled high, at which time execution continues.

**WR.** Write (Output, active Low, tri-state).  $\overline{\text{WR}}$  indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

**XTAL.** Crystal Oscillator Connection (Input, active High). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see “DC Characteristics”).

Several pins are used for different conditions, depending on the circumstance.

## Multiplexed Pin Descriptions

A18 / T <sub>OUT</sub>	During RESET, this pin is initialized as the A18 pin. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to 1, T <sub>OUT</sub> function is selected. If TOC1 and TOC0 are cleared to 0, the A18 function is selected.
CKA0 / DREQ0	During RESET, this pin is initialized as the CKA0 pin. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to 1, the DREQ0 function is always selected.
CKA1 / TEND0	During RESET, this pin is initialized as the CKA1 pin. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, the TEND0 function is selected. If the CKA1D bit is set to 0, the CKA1 function is selected.
RXS / CTS1	During RESET, this pin is initialized as RXS pin. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to 1, the CTS1 function is selected. If the CTS1E bit is set to 0, the RXS function is selected.

## ARCHITECTURE

The Z180 combines a high-performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller, Interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks: direct memory access (DMA) control (2 channels), asynchronous serial communication interface (ASCI, 2 channels) programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSIO) channel.

**Clock Generator.** This logic generates a system clock from an external crystal or clock input. The external clock is divided by 2 or 1 and times both internal and external devices.

**Bus State Controller.** This logic performs all of the status and bus-control activity associated with the CPU and some on-chip peripherals. This includes wait-state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

**Interrupt Controller.** This logic monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To maintain compatibility with the Z80 CPU, three different interrupts modes are supported.

**Memory Management Unit.** The MMU allows the user to map the memory used by the CPU (logically only 64KB) into the 1 MB addressing range supported by the Z8S180/Z8L180. The organization of the MMU object code maintains compatibility with the Z80 CPU, while offering access to an extended memory space. This is accomplished by using an effective common-area/banked-area scheme.

**Central Processing Unit.** The CPU is microcoded to provide a core that is object-code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiplication. The core has been modified to allow many of the instructions to execute in fewer clock cycles.

**DMA Controller.** The DMA controller provides high speed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory to/from I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1 MB address range with a block length up to 64 KB, and can cross over 64K boundaries.

**Asynchronous Serial Communication Interface (ASCI).** The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable

baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communication format as well as break detection and generation

**Programmable Reload Timers (PRT).** This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

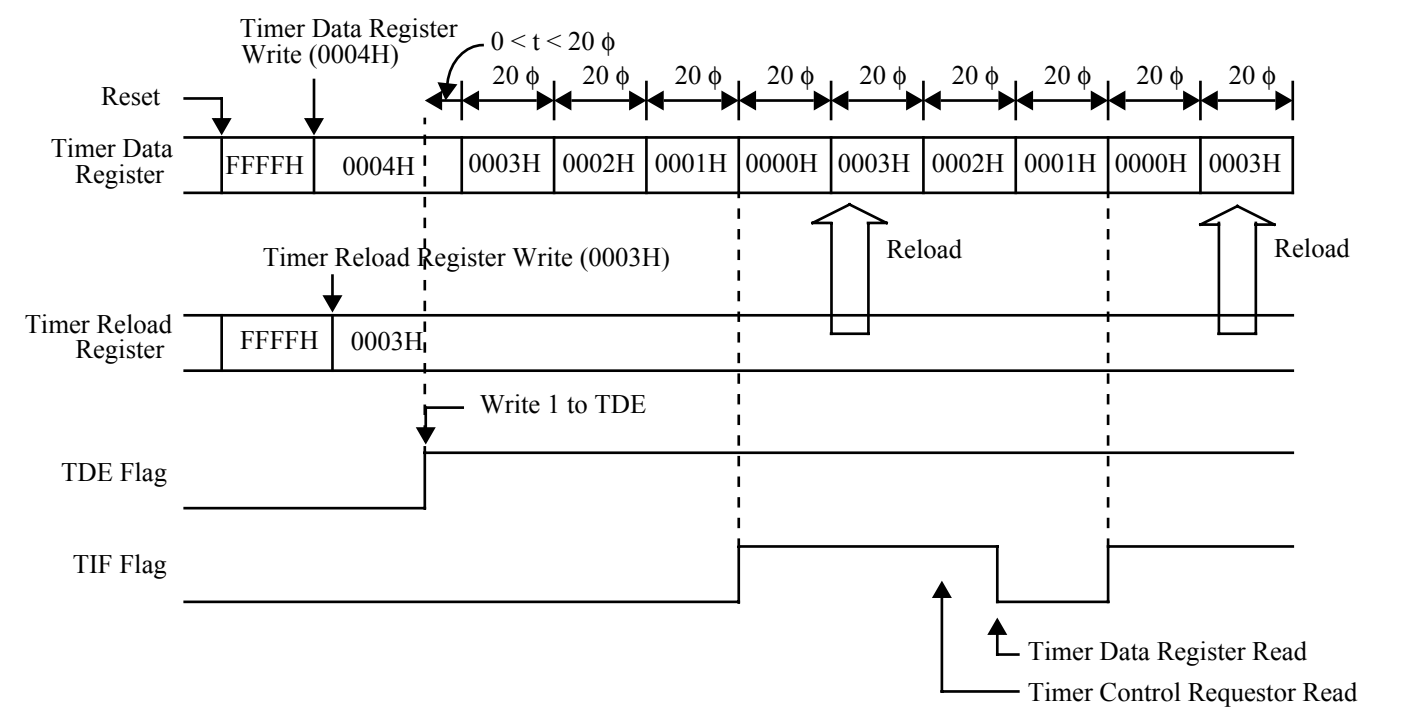


Figure 5. Timer Initialization, Count Down, and Reload Timing

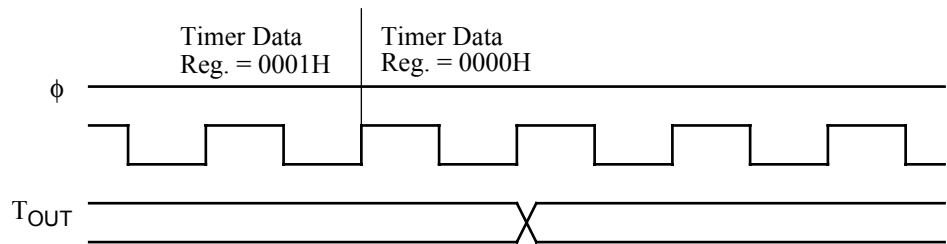


Figure 6. Timer Output Timing

**Clocked Serial I/O (CSI/O).** The CSIO channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met (Transmit and Receive operation cannot occur simul-

taneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O does not work.

**Note:** TRDR is not buffered. Performing a CSI/O transmit while the previous transmission is still in progress causes the data to be immediately updated

and corrupts the transmit operation. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

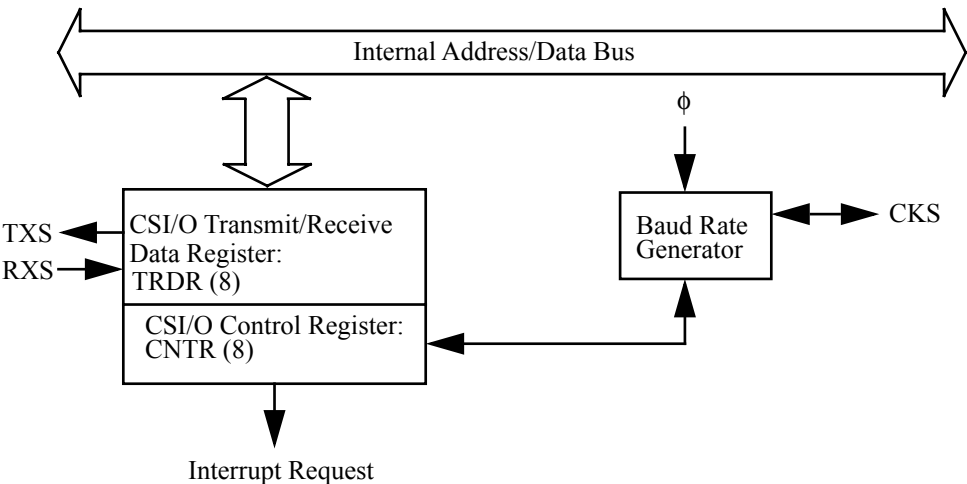


Figure 7. CSIO Block Diagram

OPERATION MODES

**Z80 versus 64180 Compatibility.** The Z8S180/Z8L180 is descended from two different “ancestor” processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR), shown in Figure 8, can be programmed to select between certain Z80 and 64180 differences.

On the Z8S180/Z8L180, this choice makes the processor fetch an RETI instruction one time. When fetching an RETI from a zero-wait-state memory location, the processor uses three clock machine cycles. Although these clock cycles are not fully Z80-timing compatible, they are compatible.

When M1E=0, the processor does not drive M1 Low during the instruction fetch cycles. After fetching an RETI instruction one time with normal timing, the processor goes back and refetches the instruction using fully Z80-compatible cycles that include driving M1 Low. This may be required by some external Z80 peripherals to properly decode the RETI instruction. Figure 9 and Table 4 show the RETI sequence when M1E=0.

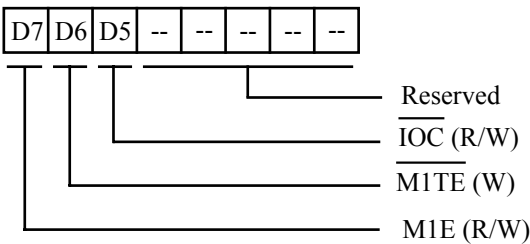


Figure 8. Operating Control Register  
(OMCR: I/O Address = 3EH)

**M1E (M1 Enable).** This bit controls the M1 output and is set to a 1 during RESET.

When M1E=1, the M1 output is asserted Low during the opcode fetch cycle, the INT0 cycle and the first machine cycle of the NMI acknowledge.

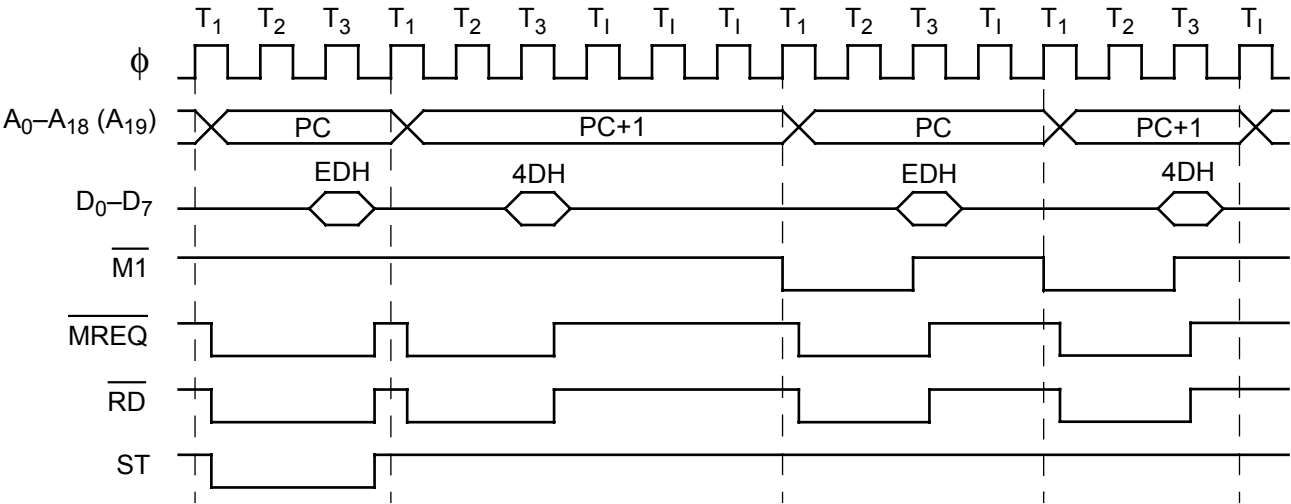


Figure 9. RETI Instruction Sequence with MIE=0

Table 4. RETI Control Signal States with MIE=0

Machine				M1							
Cycle	States	Address	Data	RD	WR	MREQ	IORQ	IOC=1	IOC=0	HALT	ST
1	T1-T3	1st Opcode	EDH	0	1	0	1	0	1	1	0
2	T1-T3	2nd Opcode	4DH	0	1	0	1	0	1	1	0
	Ti	NA	Tri-State	1	1	1	1	1	1	1	1
	Ti	NA	Tri-State	1	1	1	1	1	1	1	1
	Ti	NA	Tri-State	1	1	1	1	1	1	1	1
3	T1-T3	1st Opcode	EDH	0	1	0	1	0	0	1	1
	Ti	NA	Tri-State	1	1	1	1	1	1	1	1
4	T1-T3	2nd Opcode	4DH	0	1	0	1	0	1	1	1
5	T1-T3	SP	Data	0	1	0	1	1	1	1	1
6	T1-T3	SP+1	Data	0	1	0	1	1	1	1	1

**M1TE (M1 Temporary Enable).** This bit controls the temporary assertion of the M1 signal. It is always read back as a 1 and is set to 1 during RESET.

When M1E is set to 0 to accommodate certain external Z80 peripheral(s), those same device(s) may require a pulse on M1 after programming certain of their registers to complete the function being programmed.

For example, when a control word is written to the Z80 PIO to enable interrupts, no enable actually takes place until the PIO sees an active M1 signal. When M1TE=1, there is no change in the operation of the M1 signal, and M1E controls its function. When M1TE=0, the M1 output is asserted during the next opcode fetch cycle regardless of the state programmed into the M1E bit. This is only momentary (one time) and it is not necessary to preprogram a 1 to disable the function (see Figure10).



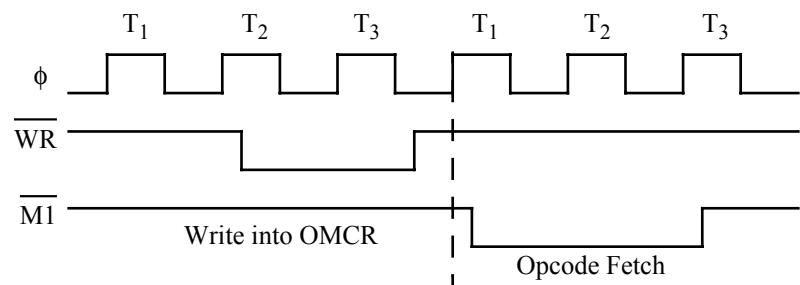


Figure 10. M1 Temporary Enable Timing

**IOC.** This bit controls the timing of the  $\overline{\text{IORQ}}$  and  $\overline{\text{RD}}$  signals. The bit is set to 1 by RESET. When  $\overline{\text{IOC}}=1$ , the  $\overline{\text{IORQ}}$  and  $\overline{\text{RD}}$  signals function the same as the Z64180 (Figure 11).

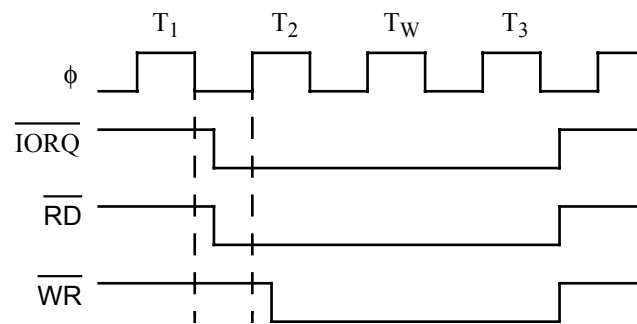


Figure 11. I/O Read and Write Cycles with IOC = 1

When  $\overline{\text{IOC}}=0$ , the timing of the  $\overline{\text{IORQ}}$  and  $\overline{\text{RD}}$  signals match the timing of the Z80. The  $\overline{\text{IORQ}}$  and  $\overline{\text{RD}}$  signals go active as a result of the rising edge of T<sub>2</sub>. (Figure 12.)

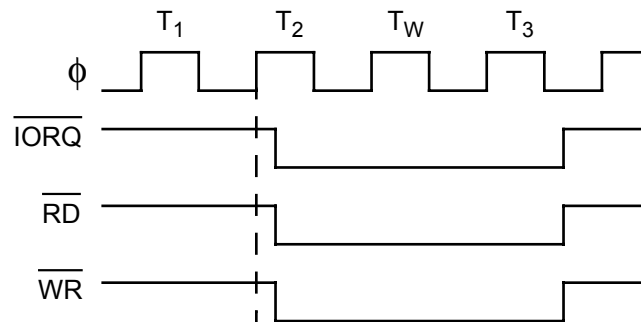


Figure 12. I/O Read and Write Cycles with IOC = 0

**HALT and Low-Power Operating Modes.** The Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

**Normal Operation.** In this state, the Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the HALT pin is High.

**HALT Mode.** This mode is entered by the HALT instruction. Thereafter, the Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it and drives the HALT, ST and M1 pins all Low. The oscillator and PHI pin remain Active. Interrupts and bus granting to external Masters, and DRAM refresh can occur, and all on-chip I/O devices continue to operate including the DMA channels.

The Z8S180/Z8L180 leaves HALT mode in response to:

- Low on RESET
- Interrupt from an enabled on-chip source
- External request on NMI
- Enabled external request on INT0, INT1, or INT2

In case of an interrupt, the return address is the instruction following the HALT instruction. The program can either branch back to the HALT instruction to wait for another interrupt or can examine the new state of the system/application and respond appropriately

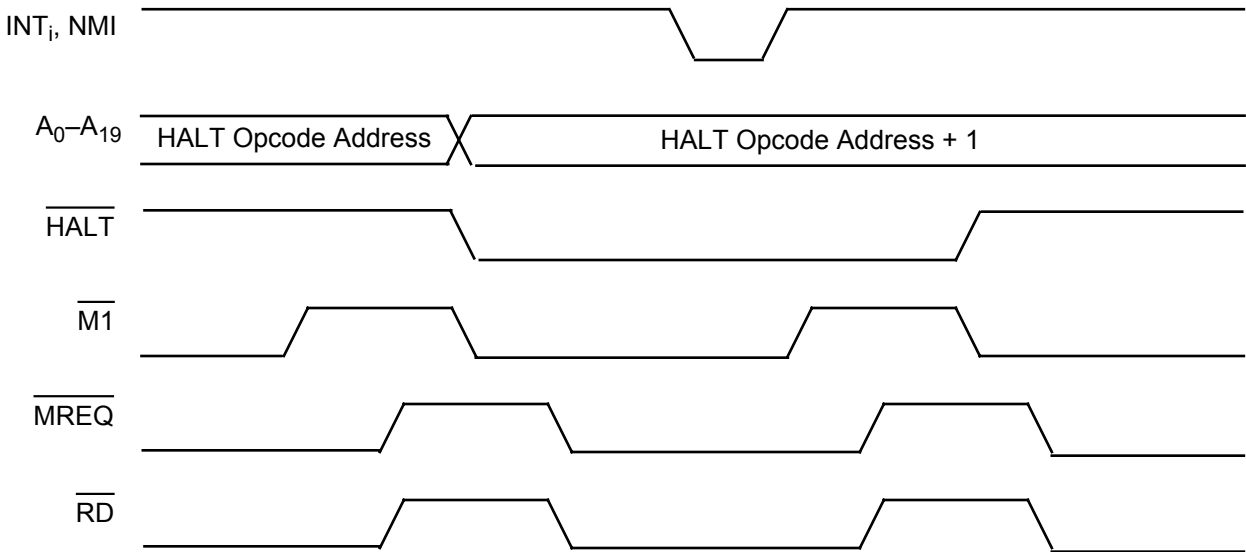


Figure 13. HALT Timing

**SLEEP Mode.** This mode is entered by keeping the IOSTOP bit (ICR5) and bits 3 and 6 of the CPU Control Register (CCR3, CCR6) all zero and executing the SLP instruction. The oscillator and PHI output continue operating, but are blocked from the CPU core and DMA channels to reduce power consumption. DRAM refresh stops, but interrupts and granting to an external Master can occur.

Except when the bus is granted to an external Master, A19-0 and all control signals except HALT are maintained High. HALT is Low. I/O operations continue as before the SLP instruction, except for the DMA channels.

The Z8S180/Z8L180 leaves SLEEP mode in response to a low on RESET, an interrupt request from an on-chip source, an external request on NMI, or an external request on INT0, INT1, or INT2.

If an interrupt source is individually disabled, it cannot bring the Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 1 so that interrupts are globally enabled (by an EI instruction), the highest priority active interrupt occurs with the return address being the instruction after the SLP instruction. If

an interrupt source is individually enabled, but the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s).

This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request. Note that the Z8S180/Z8L180 takes about 1.5 clock ticks to restart.

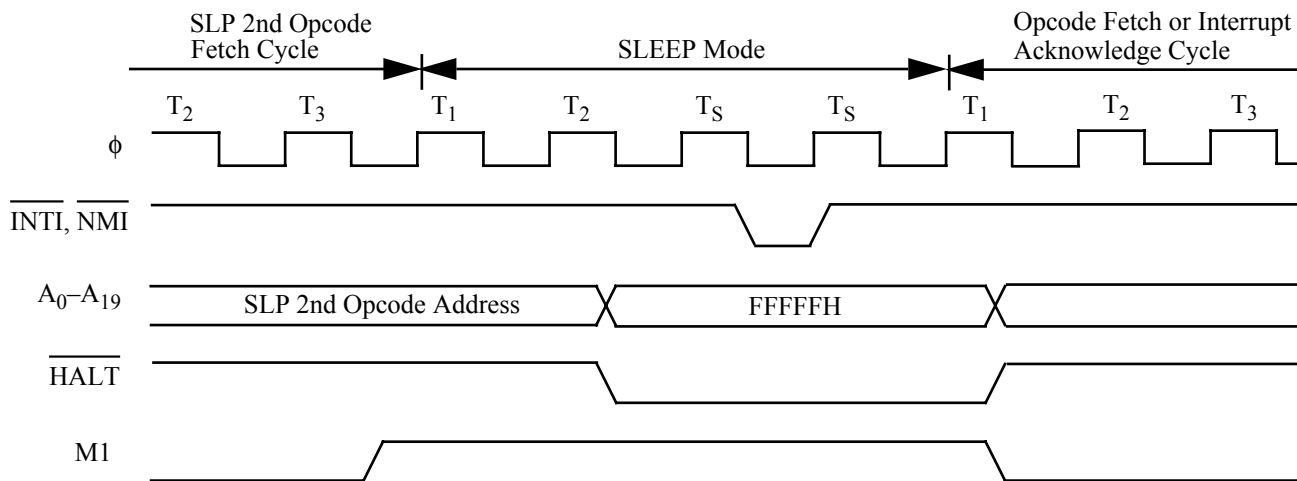


Figure 14. SLEEP Timing

**IOSTOP Mode.** IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

**SYSTEM STOP Mode.** SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

**IDLE Mode.** Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

- Set the IOSTOP bit (ICR5) to 1
- Set CCR6 to 0

- Set CCR3 to 1
- Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on RESET, an external interrupt request on NMI, or an external interrupt request on INT0, INT1 or INT2 that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an NMI, or due to an enabled external interrupt request when the IEF flag is 1 due to an EI instruction, it starts by performing the interrupt with the return address being that of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves

IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

**Note:** The Z8S180/Z8L180 takes about 9.5 clocks to restart.

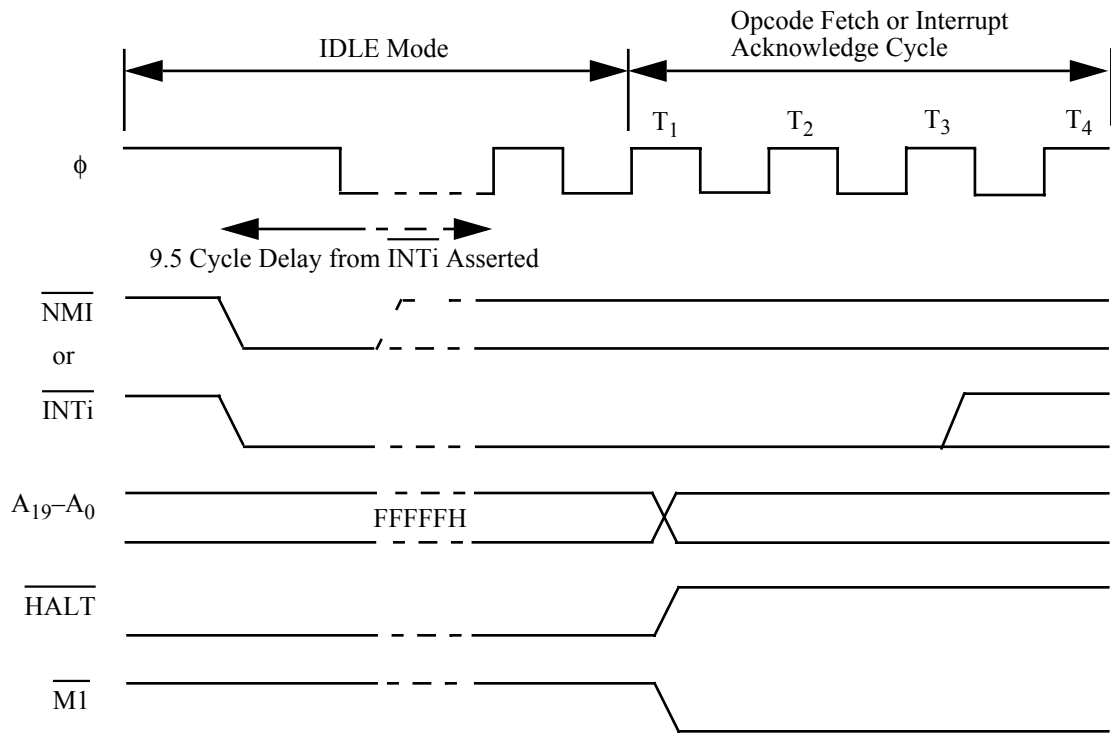


Figure 15. Z8S180/Z8L180 IDLE Mode Exit due to External Interrupt

While the Z8S180/Z8L180 is in IDLE mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 16 depicts the timing for this sequence.

**Note:** A response to a bus request takes 8 clock cycles longer than in normal operation.

After the external Master negates the Bus Request, the Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

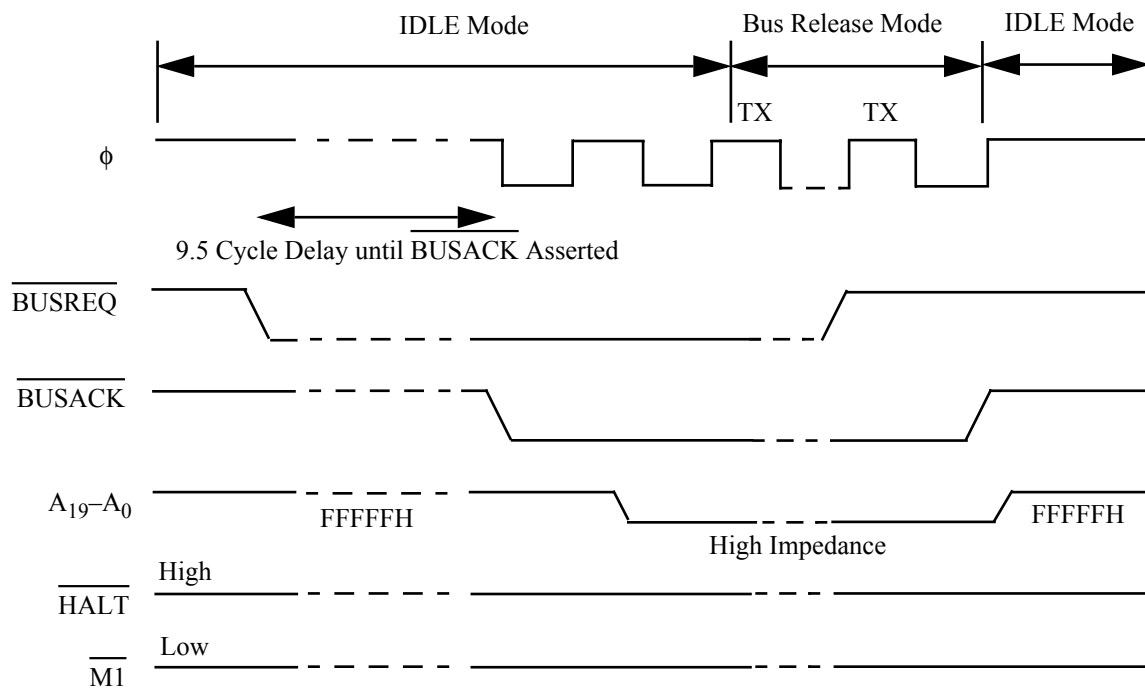


Figure 16. Bus Granting to External Master in IDLE Mode

**STANDBY Mode (With or Without QUICK RECOVERY).** Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on RESET, on NMI, or a Low on INT0-2 that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity to restart the on-chip oscillator and ensure that it has stabilized to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding HALT Low and M1 High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives RESET Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source has been stopped, the external logic must hold RESET Low until the on-chip oscillator or external clock source has restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

- Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode
- Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits 217 (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called

QUICK RECOVERY mode. The same delay applies to granting the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to NMI Low or an enabled INTO-INT2 low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in

the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If INT0, or INT1 or INT2 goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request. Note that the Z8S180/Z8L180 takes either 64 or 217 (131,072) clocks to restart, depending on the CCR3 bit.

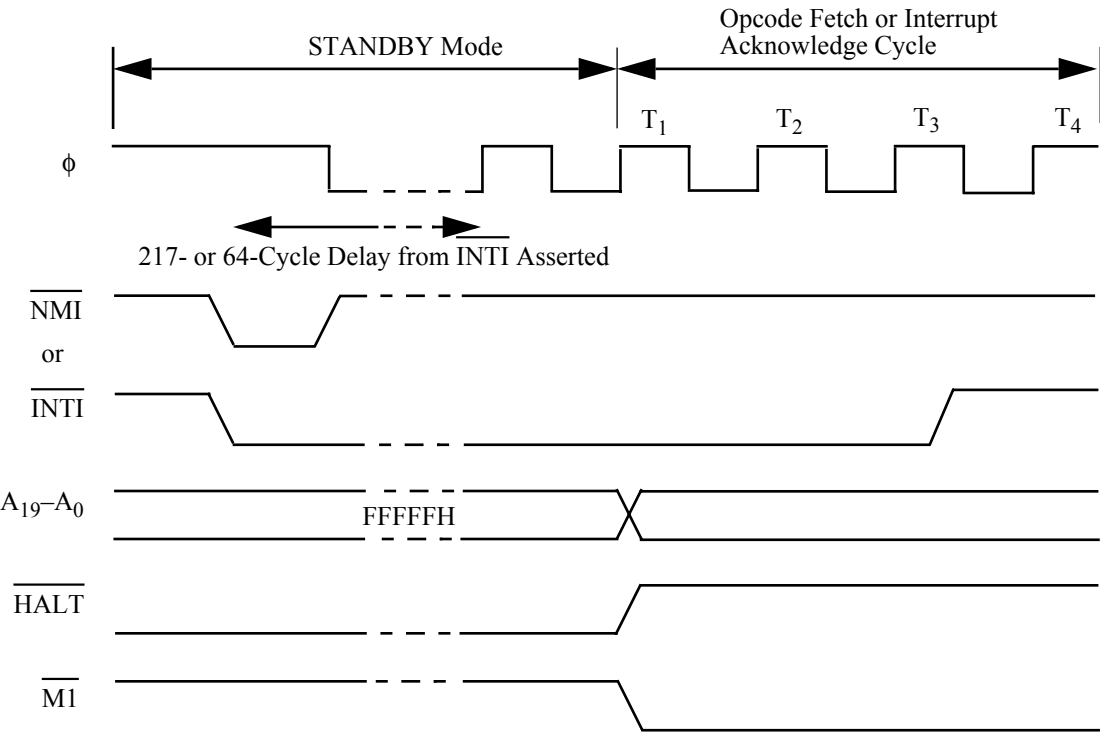


Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 217 (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (not the Quick Recovery) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

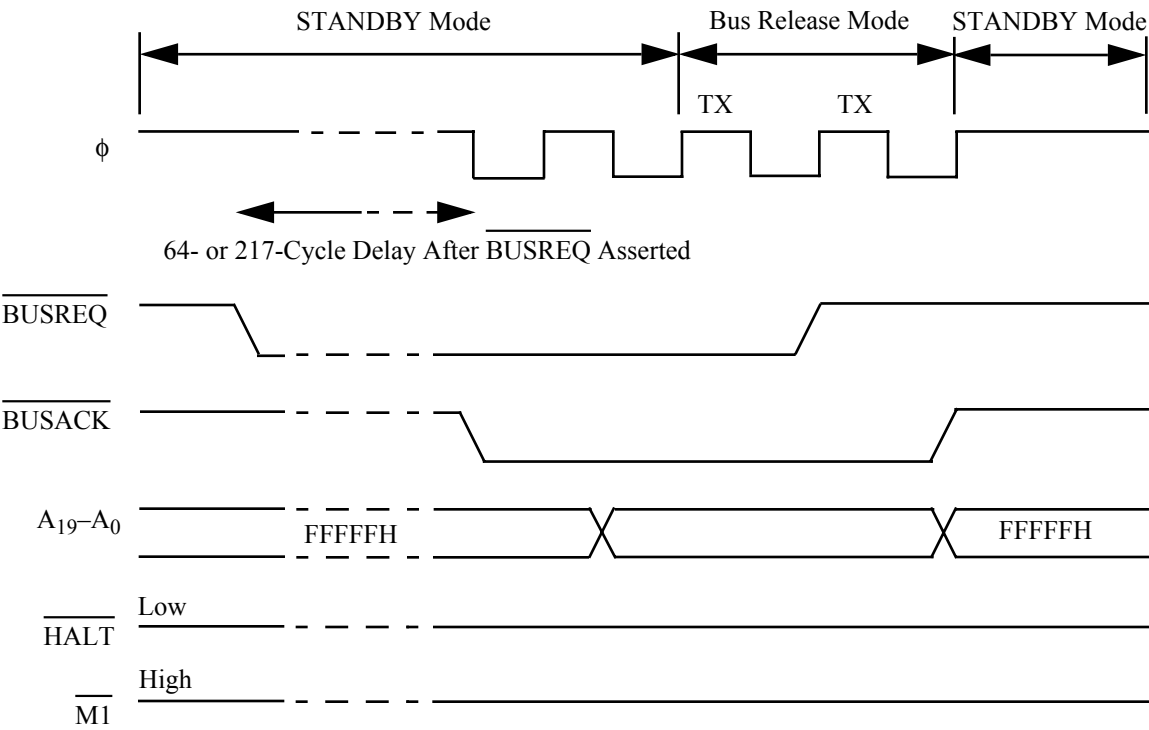


Figure 18. Bus Granting to External Master During STANDBY Mode

STANDARD TEST CONDITIONS

The “DC Characteristics” and “Capacitance” sections apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points). The “Ordering Information” section lists temperature ranges and product numbers. Package drawings are in the Package Information section.

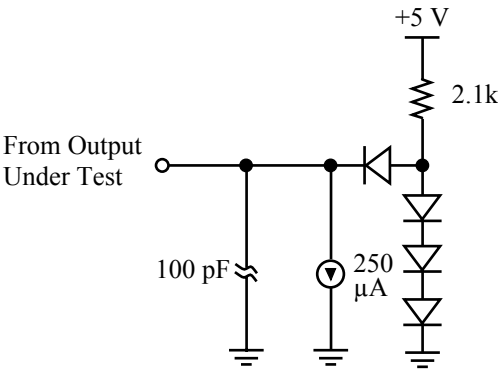


Figure 19. AC Load Capacitance Parameters

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	−0.3 ~ +7.0	V
Input Voltage	V <sub>IN</sub>	−0.3 ~ V <sub>CC</sub> +0.3	V
Operating Temperature	T <sub>OPR</sub>	0 ~ 70	°C
Extended Temperature	T <sub>EXT</sub>	−40 ~ 85	°C
Storage Temperature	T <sub>STG</sub>	−55 ~ +150	°C

**Note:** Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.



**DC CHARACTERISTICS - S180**

$V_{CC} = 5V + 10\%$ ,  $V_{SS} = 0V$  over the specified temperature range  
unless otherwise noted.

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
$V_{IH1}$	Input H Voltage RESET, EXTAL, NMI		$V_{CC} - 0.6$	–	$V_{CC} + 0.3$	V
$V_{IH2}$	Input H Voltage Except RESET, EXTAL, NMI		2.0	–	$V_{CC} + 0.3$	V
$V_{IH3}$	Input H Voltage Except CKS, CKA0, CKA1		2.4	–	$V_{CC} + 0.3$	V
$V_{IL1}$	Input L Voltage RESET, EXTAL, NMI		–0.3	–	0.6	V
$V_{IL2}$	Input L Voltage Except RESET, EXTAL, NMI		–0.3	–	0.8	V
$V_{OH}$	Outputs H Voltage All outputs	$I_{OH} = -200 \mu A$	2.4	–	–	V
		$I_{OH} = -20 \mu A$	$V_{CC} - 1.2$	–	–	
$V_{OL}$	Outputs L Voltage All outputs	$I_{OL} = -2.2 \text{ mA}$	–	–	0.45	V
$I_{IL}$	Input Leakage Current All Inputs Except XTAL, EXTAL	$V_{IN} = 0.5 \sim V_{CC} - 0.5$	–	–	1.0	$\mu A$
$I_{TL}$	Three State Leakage Current	$V_{IN} = 0.5 \sim V_{CC} - 0.5$	–	–	1.0	$\mu A$
$I_{CC}^1$	Power Dissipation (Normal Operation)	F = 10 MHz	–	25	60	mA
		20		30	50	
		33		60	100	
	Power Dissipation (SYSTEM STOP mode)	F = 10 MHz	–	2	5	
		20		3	6	
		33		5	9	
$C_P$	Pin Capacitance	$V_{IN} = 0_V$ , f = 1 MHz $T_a = 25^\circ \text{C}$	–	–	12	pF

**Note:**

1.  $V_{IHmin} = V_{CC} - 1.0V$ ,  $V_{ILmax} = 0.8V$  (All output terminals are at NO LOAD.)  $V_{CC} = 5.0V$

## DC CHARACTERISTICS - Z8L180

$V_{CC} = 5V + 10\%$ ,  $V_{SS} = 0V$  over the specified temperature range  
unless otherwise noted.

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
$V_{IH1}$	Input H Voltage RESET, EXTAL, NMI		$V_{CC} - 0.6$		$V_{CC} + 0.3$	V
$V_{IH2}$	Input H Voltage Except RESET, EXTAL, NMI		2.0		$V_{CC} + 0.3$	V
$V_{IL1}$	Input L Voltage RESET, EXTAL, NMI		-0.3		0.6	V
$V_{IL2}$	Input L Voltage Except RESET, EXTAL, NMI		-0.3		0.8	V
$V_{OH1}$	Outputs H Voltage All outputs	$I_{OH} = -200 \mu A$	2.15			V
$V_{OH2}$	Outputs H Voltage	$I_{OH} = -200 \mu A$	$V_{CC} - 0.6$			V
$V_{OL1}$	Outputs L VOLTAGE ALL OUTPUTS	$I_{OL} = 4 \text{ mA}$			0.4	V
$V_{OL2}$	Outputs L PHI	$I_{OL} = 4 \text{ mA}$			0.4	V
$I_{IL}$	Input Leakage Current All Inputs Except XTAL, EXTAL	$V_{IN} = 0.5 \sim V_{CC} - 0.5$			1.0	$\mu A$
$I_{TL}$	Three State Leakage Current	$V_{IN} = 0.5 \sim V_{CC} - 0.5$			1.0	$\mu A$
$I_{CC}$	Power Dissipation (Normal Operation)	$F = 20 \text{ MHz}$		30	60	MA
	Power Dissipation (SYSTEM STOP mode)	$F = 20 \text{ MHz}$		5	10	
$I_{CC}$	Power Dissipation (Normal Operation)	$F = 20 \text{ MHz}$		30	60	MA
	Power Dissipation (SYSTEM STOP mode)	$F = 20 \text{ MHz}$		5	10	
$C_P$	Pin Capacitance	$V_{IN} = 0_V, f = 1 \text{ MHz}$ $T_a = 25^\circ \text{ C}$			12	pF

**Note:**

1.  $V_{IHmin} = V_{CC} - 1.0V$ ,  $V_{ILmax} = 0.6V$  (All output terminals are at NO LOAD.)  $V_{CC} = 3.0V$

## AC CHARACTERISTICS

$V_{CC} = 5V + 10\%$ ,  $V_{SS} = 0V$ ,  $T_A$  0 to +70° C, unless otherwise noted.

			Z8S180–10 MHz		
No.	Symbol	Item	Min.	Max.	Unit
1.	$t_{cyc}$	Clock Cycle Time	100	2000	ns
2.	$t_{CHW}$	Clock H Pulse Width	40	–	ns
3.	$t_{CLW}$	Clock L Pulse Width	40	–	ns
4.	$t_{cf}$	Clock Fall Time	–	10	ns
5.	$t_{cr}$	Clock Rise Time	–	10	ns
6.	$t_{AD}$	Ø Rise to Address Valid Delay	–	70	ns
7.	$t_{AS}$	Address Valid to MREQ Fall or IORQ Fall)	10	–	ns
8.	$t_{MED1}$	Ø Fall to MREQ Fall Delay	–	50	ns
9.	$t_{RDD1}$	Ø Fall to RD Fall Delay $\overline{IO\overline{C}} = 1$	–	50	ns
		Ø Rise to RD Rise Delay $\overline{IO\overline{C}} = 0$	–	55	
10.	$t_{M1D1}$	Ø Rise to M1 Fall Delay	–	60	ns
11.	$t_{AH}$	Address Hold Time from (MREQ, /IOREQ, RD, WR)	10	–	ns
12.	$t_{MED2}$	Ø Fall to MREQ Rise Delay	–	50	ns
13.	$t_{RDD2}$	Ø Fall to RD Rise Delay	–	50	ns
14.	$t_{M1D2}$	Ø Rise to M1 Rise Delay	–	60	ns
15.	$t_{DRS}$	Data Read Set-up Time	25	–	ns
16.	$t_{DRH}$	Data Read Hold Time	0	–	ns
17.	$t_{STD1}$	Ø Fall to ST Fall Delay	–	60	ns
18.	$t_{STD2}$	Ø Fall to ST Rise Delay	–	60	ns
19.	$t_{WS}$	WAIT Set-up Time to Ø Fall	30	–	ns
20.	$t_{WH}$	WAIT Hold Time from Ø Fall	30	–	ns
21.	$t_{WDZ}$	Ø Rise to Data Float Delay	–	60	ns
22.	$t_{WRD1}$	Ø Rise to WR Fall Delay	–	50	ns
23.	$t_{WDD}$	Ø Fall to Write Data Delay Time	–	60	ns
24.	$t_{WDS}$	Write Data Set-up Time to WR Fall	15	–	ns
25.	$t_{WRD2}$	Ø Fall to WR Rise Delay	–	50	ns
26.	$t_{WRP}$	WR Pulse Width	110	–	ns
26a.		WR Pulse Width (I/O Write Cycle)	210	–	ns
27.	$t_{WDH}$	Write Data Hold Time from (WR Rise)	10	–	ns
28.	$t_{IOD1}$	Ø Fall to IORQ Fall Delay $\overline{IO\overline{C}} = 1$	–	50	ns
		Ø Rise to IORQ Fall Delay $\overline{IO\overline{C}} = 1$	–	55	
29.	$t_{IOD2}$	Ø Fall to IORQ Rise Delay	–	50	ns

			<b>Z8S180–10 MHz</b>		
<b>No.</b>	<b>Symbol</b>	<b>Item</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
30.	$t_{IOD3}$	M1 Fall to IORQ Fall Delay	200	–	ns
31.	$t_{INTS}$	/INT Set-up Time to $\emptyset$ Fall	30	–	ns
32.	$t_{INTS}$	/INT Hold Time from $\emptyset$ Fall	30	–	ns
33.	$t_{NMIW}$	NMI Pulse Width	80	–	ns
34.	$t_{BRS}$	BUSREQ Set-up Time to $\emptyset$ Fall	30	–	ns
35.	$t_{BRH}$	BUSREQ Hold Time from $\emptyset$ Fall	30		ns
36.	$t_{BAD1}$	$\emptyset$ Rise to BUSACK Fall Delay	–	60	ns
37.	$t_{BAD2}$	$\emptyset$ Fall to BUSACK Rise Delay	–	60	ns
38.	$t_{BZD}$	$\emptyset$ Rise to Bus Floating Delay Time	–	80	ns
39.	$t_{MEWH}$	MREQ Pulse Width (HIGH)	70	–	ns
40.	$t_{MEWL}$	MREQ Pulse Width (LOW)	80	–	ns
41.	$t_{RFD1}$	$\emptyset$ Rise to RFSH Fall Delay	–	60	ns
42.	$t_{RFD2}$	$\emptyset$ Rise to RFSH Rise Delay	–	60	ns
43.	$t_{HAD1}$	$\emptyset$ Rise to HALT Fall Delay	–	50	ns
44.	$t_{HAD2}$	$\emptyset$ Rise to HALT Rise Delay	–	50	ns
45.	$t_{DRQS}$	$\overline{DREQ_i}$ Set-up Time to $\emptyset$ Rise	30	–	ns
46.	$t_{DRQH}$	$\overline{DREQ_i}$ Hold Time from $\emptyset$ Rise	30	–	ns
47.	$t_{TED1}$	$\emptyset$ Fall to $\overline{TEND_i}$ Fall Delay	–	50	ns
48.	$t_{TED2}$	$\emptyset$ Fall to $\overline{TEND_i}$ Rise Delay	–	50	ns
49.	$t_{ED1}$	$\emptyset$ Rise to E Rise Delay	–	60	ns
50.	$t_{ED2}$	$\emptyset$ Fall or Rise to E Fall Delay	–	60	ns
51.	$P_{WEH}$	E Pulse Width (HIGH)	55	–	ns
52.	$P_{WEL}$	E Pulse Width (LOW)	110	–	ns
53.	$t_{Er}$	Enable Rise Time	–	20	ns
54.	$t_{Ef}$	Enable Fall Time	–	20	ns
55.	$t_{TOD}$	$\emptyset$ Fall to Timer Output Delay	–	150	ns
56.	$t_{STDI}$	CSI/O Transmit Data Delay Time (Internal Clock Operation)	–	150	ns
57.	$t_{STDE}$	CSI/O Transmit Data Delay Time (External Clock Operation)	–	7.5tcyc +150	ns
58.	$t_{SRSI}$	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	–	tcyc
59.	$t_{SRHI}$	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	–	tcyc
60.	$t_{SRSE}$	CSI/O Receive Data Set-up Time (External Clock Operation)	1	–	tcyc

			Z8S180–10 MHz		
No.	Symbol	Item	Min.	Max.	Unit
61.	$t_{SRHE}$	CSI/O Receive Data Hold Time (External Clock Operation)	1	–	tcyc
62.	$t_{RES}$	RESET Set-up Time to $\emptyset$ Fall	80	–	ns
63.	$t_{REH}$	RESET Hold Time from $\emptyset$ Fall	50	–	ns
64.	$t_{OSC}$	Oscillator Stabilization Time	–	TBD	ns
65.	$t_{EXr}$	External Clock Rise Time (EXTAL)	–	25	ns
66.	$t_{EXf}$	External Clock Fall Time (EXTAL)	–	25	ns
67.	$t_{Rr}$	RESET Rise Time	–	50	ns
68.	$t_{Rf}$	RESET Fall Time	–	50	ns
69.	$t_{Ir}$	Input Rise Time (except EXTAL, RESET)	–	100	ns
70.	$t_{If}$	Input Fall Time (except EXTAL, RESET)	–	100	ns

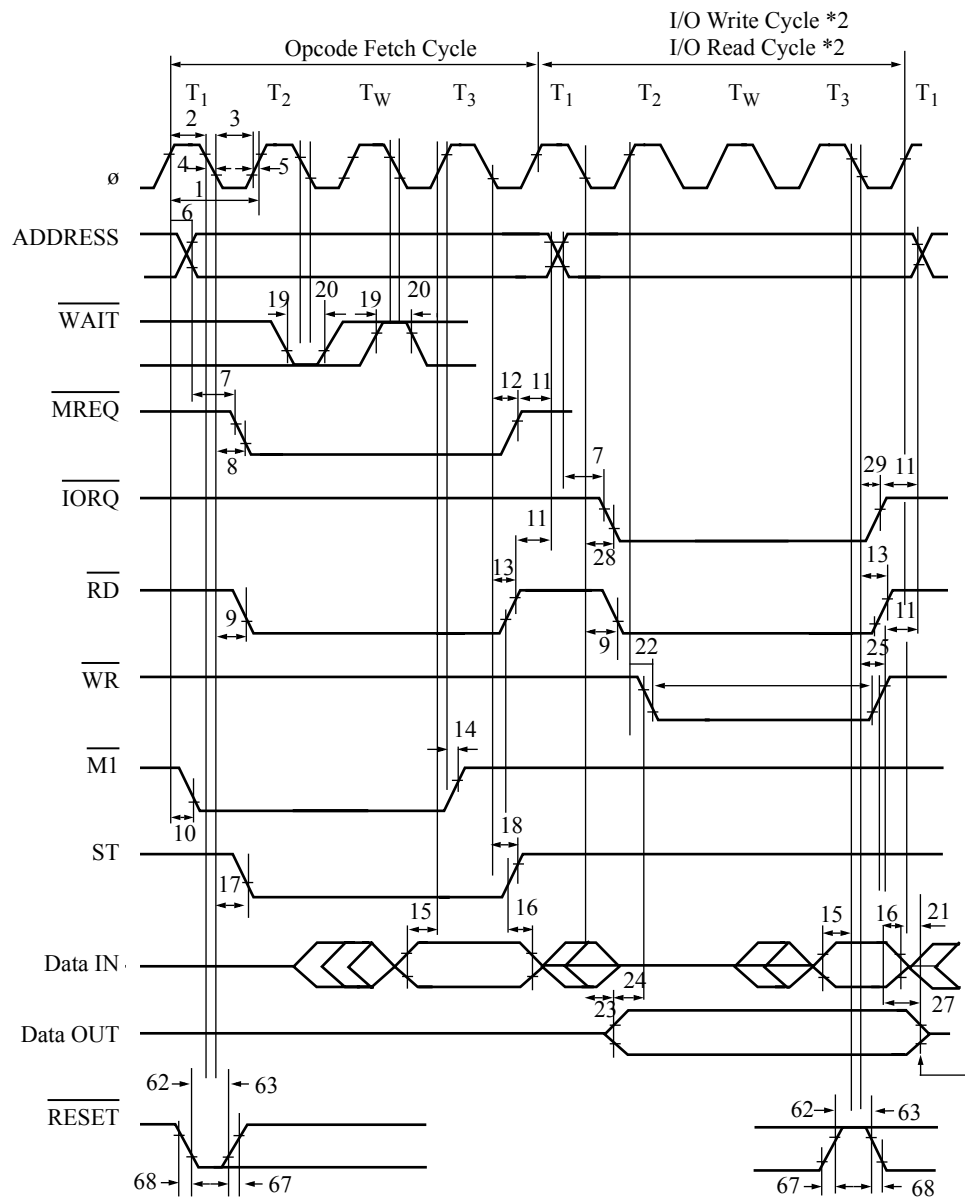
( $V_{CC} = 5V \pm 10\%$  or  $V_{CC} = 3.3V \pm 10\%$  over specified temperature range, unless otherwise noted, 33-MHz characteristics apply only to 5V operation.)

			Z8S180–20 MHz		Z8S180–33 MHz		Unit
No.	Symbol	Item	Min.	Max.	Min.	Max.	
1.	$t_{CYC}$	Clock Cycle Time	50	2000	33	2000	ns
2.	$t_{CHW}$	Clock “H” Pulse Width	15	–	10	–	ns
3.	$t_{CLW}$	Clock “L” Pulse Width	15	–	10	–	ns
4.	$t_{CF}$	Clock Fall Time	–	10	–	5	ns
5.	$t_{CR}$	Clock Rise Time	–	10	–	5	ns
6.	$t_{AD}$	$\emptyset$ Rise to Address Valid Delay	–	15	–	15	ns
7.	$t_{AS}$	Address Valid to MREQ Fall or IORQ Fall)	20	–	5	–	ns
8.	$t_{MED1}$	$\emptyset$ Fall to MREQ Fall Delay	–	15	–	15	ns
9.	$t_{RDD1}$	$\emptyset$ Fall to RD Fall Delay $\overline{IO\overline{C}} = 1$	–	15	–	15	ns
		$\emptyset$ Rise to RD Rise Delay $\overline{IO\overline{C}} = 0$	–	15	–	15	
10.	$t_{M1D1}$	$\emptyset$ Rise to M1 Fall Delay	–	15	–	15	ns
11.	$t_{AH}$	Address Hold Time from (MREQ, /IOREQ, RD, WR)	20	–	20	–	ns
12.	$t_{MED2}$	$\emptyset$ Fall to MREQ Rise Delay	–	15	–	15	ns
13.	$t_{RDD2}$	$\emptyset$ Fall to RD Rise Delay	–	15	–	15	ns
14.	$t_{M1D2}$	$\emptyset$ Rise to M1 Rise Delay	–	15	–	15*	ns
15.	$t_{DRS}$	Data Read Set-up Time	15	–	15	–	ns
16.	$t_{DRH}$	Data Read Hold Time	0	–	0	–	ns

No.	Symbol	Item	Z8S180–20 MHz		Z8S180–33 MHz		Unit
			Min.	Max.	Min.	Max.	
17.	$t_{STD1}$	$\emptyset$ Fall to ST Fall Delay	–	15	–	15	ns
18.	$t_{STD2}$	$\emptyset$ Fall to ST Rise Delay	–	15	–	15	ns
19.	$t_{WS}$	WAIT Set-up Time to $\emptyset$ Fall	15	–	15	–	ns
20.	$t_{WH}$	WAIT Hold Time from $\emptyset$ Fall	5	–	5	–	ns
21.	$t_{WDZ}$	$\emptyset$ Rise to Data Float Delay	–	10	–	10	ns
22.	$t_{WRD1}$	$\emptyset$ Rise to WR Fall Delay	–	15	–	15	ns
23.	$t_{WDD}$	$\emptyset$ Fall to Write Data Delay Time	–	20	–	20	ns
24.	$t_{WDS}$	Write Data Set-up Time to WR Fall	10	–	10	–	ns
25.	$t_{WRD2}$	$\emptyset$ Fall to WR Rise Delay	–	15	–	15	ns
26.	$t_{WRP}$	WR Pulse Width	70	–	40	–	ns
26a.		WR Pulse Width (I/O Write Cycle)	120	–	70	–	ns
27.	$t_{WDH}$	Write Data Hold Time from (WR Rise)	5	–	5	–	
28.	$t_{IOD1}$	$\emptyset$ Fall to IORQ Fall Delay $\overline{IOC} = 1$	–	15	–	15	ns
		$\emptyset$ Rise to IORQ Fall Delay $\overline{IOC} = 1$	–	15	–	15	
29.	$t_{IOD2}$	$\emptyset$ Fall to IORQ Rise Delay	–	15	–	15	ns
30.	$t_{IOD3}$	M1 Fall to IORQ Fall Delay	120	–	70	–	ns
31.	$t_{INTS}$	$\overline{INT}$ Set-up Time to $\emptyset$ Fall†	15	–	15	–	ns
32.	$t_{INTS}$	INT Hold Time from $\emptyset$ Fall	10	–	10	–	ns
33.	$t_{NMIW}$	NMI Pulse Width	35	–	25	–	ns
34.	$t_{BRS}$	BUSREQ Set-up Time to $\emptyset$ Fall	10	–	10	–	ns
35.	$t_{BRH}$	BUSREQ Hold Time from $\emptyset$ Fall	10	–	10		ns
36.	$t_{BAD1}$	$\emptyset$ Rise to BUSACK Fall Delay	–	15	–	15	ns
37.	$t_{BAD2}$	$\emptyset$ Fall to BUSACK Rise Delay	–	15	–	15	ns
38.	$t_{BZD}$	$\emptyset$ Rise to Bus Floating Delay Time	–	10	–	25	ns
39.	$t_{MEWH}$	MREQ Pulse Width (HIGH)	45	–	25	–	ns
40.	$t_{MEWL}$	MREQ Pulse Width (LOW)	45	–	25	–	ns
41.	$t_{RFD1}$	$\emptyset$ Rise to RFSH Fall Delay	–	15	–	15	ns
42.	$t_{RFD2}$	$\emptyset$ Rise to RFSH Rise Delay	–	15	–	15	ns
43.	$t_{HAD1}$	$\emptyset$ Rise to HALT Fall Delay	–	15	–	15	ns
44.	$t_{HAD2}$	$\emptyset$ Rise to HALT Rise Delay	–	15	–	15	ns
45.	$t_{DRQS}$	$\overline{DREQi}$ Set-up Time to $\emptyset$ Rise	20	–	20	–	ns
46.	$t_{DRQH}$	$\overline{DREQi}$ Hold Time from $\emptyset$ Rise	15	–	15	–	ns
47.	$t_{TED1}$	$\emptyset$ Fall to $\overline{TENDi}$ Fall Delay	–	15	–	15	ns
48.	$t_{TED2}$	$\emptyset$ Fall to $\overline{TENDi}$ Rise Delay	–	15	–	15	ns

No.	Symbol	Item	Z8S180–20 MHz		Z8S180–33 MHz		Unit
			Min.	Max.	Min.	Max.	
49.	$t_{ED1}$	Ø Rise to E Rise Delay	–	15	–	15	ns
50.	$t_{ED2}$	Ø Fall or Rise to E Fall Delay	–	15	–	15	ns
51.	$P_{WEH}$	E Pulse Width (HIGH)	45	–	20	–	ns
52.	$P_{WEL}$	E Pulse Width (LOW)	70	–	20	–	ns
53.	$t_{Er}$	Enable Rise Time	–	10	–	10	ns
54.	$t_{Ef}$	Enable Fall Time	–	10	–	10	ns
55.	$t_{TOD}$	Ø Fall to Timer Output Delay	–	50	–	50	ns
56.	$t_{STDI}$	CSI/O Transmit Data Delay Time (Internal Clock Operation)	–	2	–	2	ns
57.	$t_{STDE}$	CSI/O Transmit Data Delay Time (External Clock Operation)	–	7.5tcyc +75	–	7.5tcyc +60	ns
58.	$t_{SRSI}$	CSI/O Receive Data Set-up Time (Internal Clock Operation)	–	1	–	1	tcyc
59.	$t_{SRHI}$	CSI/O Receive Data Hold Time (Internal Clock Operation)	–	1	–	1	tcyc
60.	$t_{SRSE}$	CSI/O Receive Data Set-up Time (External Clock Operation)	–	1	–	1	tcyc
61.	$t_{SRHE}$	CSI/O Receive Data Hold Time (External Clock Operation)	–	1	–	1	tcyc
62.	$t_{RES}$	RESET Set-up Time to Ø Fall	25	–	25	–	ns
63.	$t_{REH}$	RESET Hold Time from Ø Fall	15	–	15	–	ns
64.	$t_{OSC}$	Oscillator Stabilization Time	–	20	–	20	ns
65.	$t_{EXR}$	External Clock Rise Time (EXTAL)	–	10	–	5	ns
66.	$t_{EXF}$	External Clock Fall Time (EXTAL)	–	10	–	5	ns
67.	$t_{RR}$	RESET Rise Time	–	50	–	50	ns
68.	$t_{RF}$	RESET Fall Time	–	50	–	50	ns
69.	$t_{IR}$	Input Rise Time (except EXTAL, RESET)	–	50	–	50	ns
70.	$t_{IF}$	Input Fall Time (except EXTAL, RESET)	–	50	–	50	ns

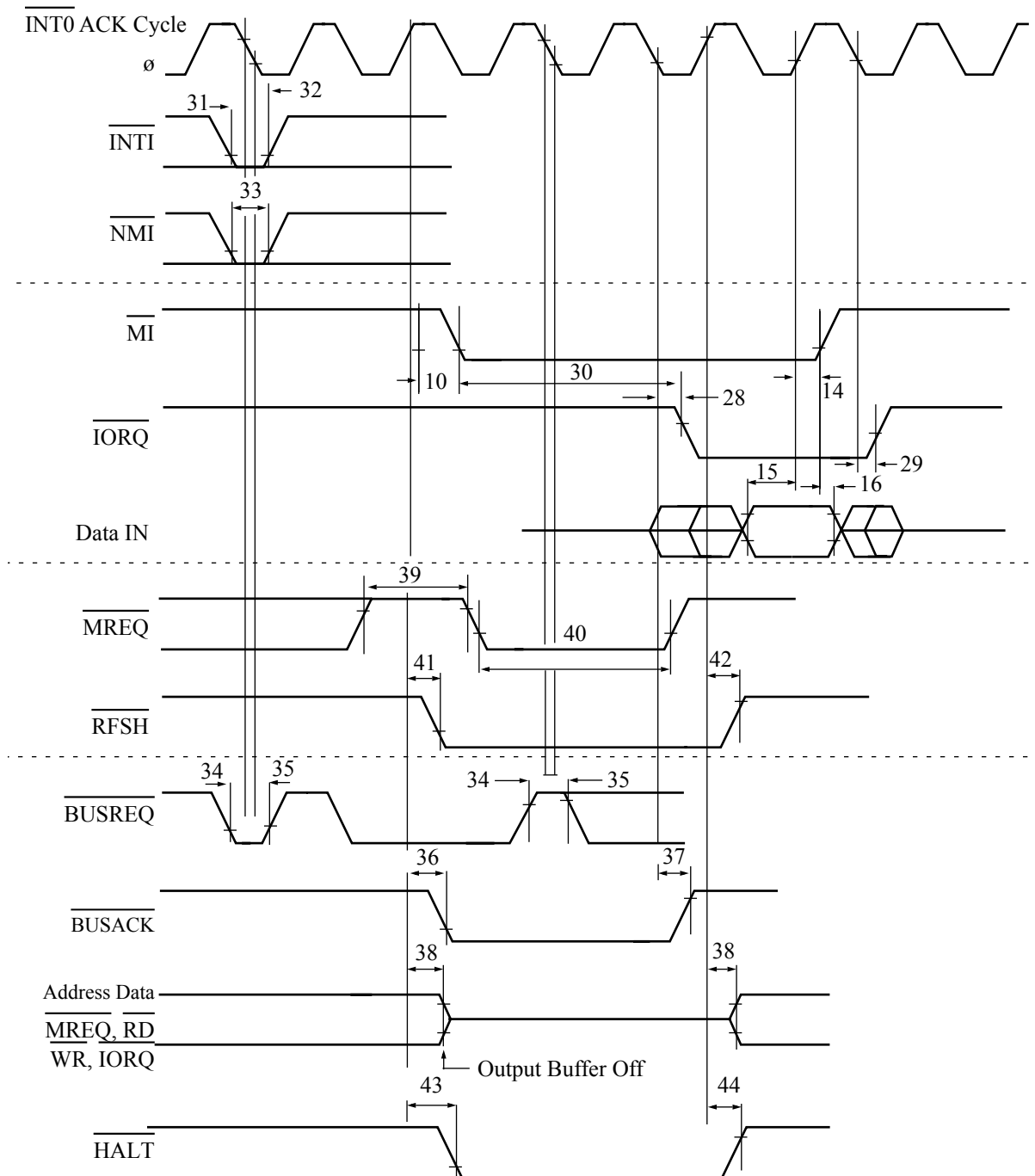
## TIMING DIAGRAMS



**Figure 20. CPU Timing**  
(Opcode Fetch Cycle, Memory Read Cycle,  
Memory Write Cycle, I/O Write Cycle, I/O Read Cycle)

**Note:** Memory Read/Write Cycle timing are the same as I/O Read/Write Cycle except there are no automatic wait states ( $T_W$ ), and MREQ is active instead of IORQ.





**Figure 21. CPU Timing**  
(INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode,  
HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

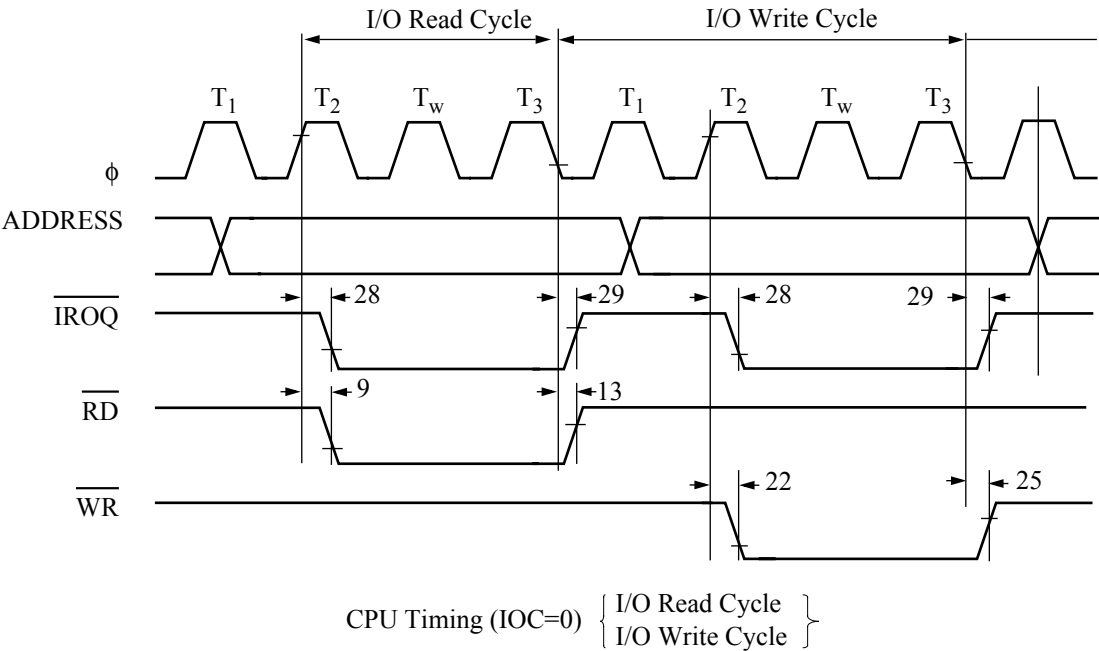


Figure 22. CPU Timing (/IOC = 0)  
(I/O Read Cycle, I/O Write Cycle)

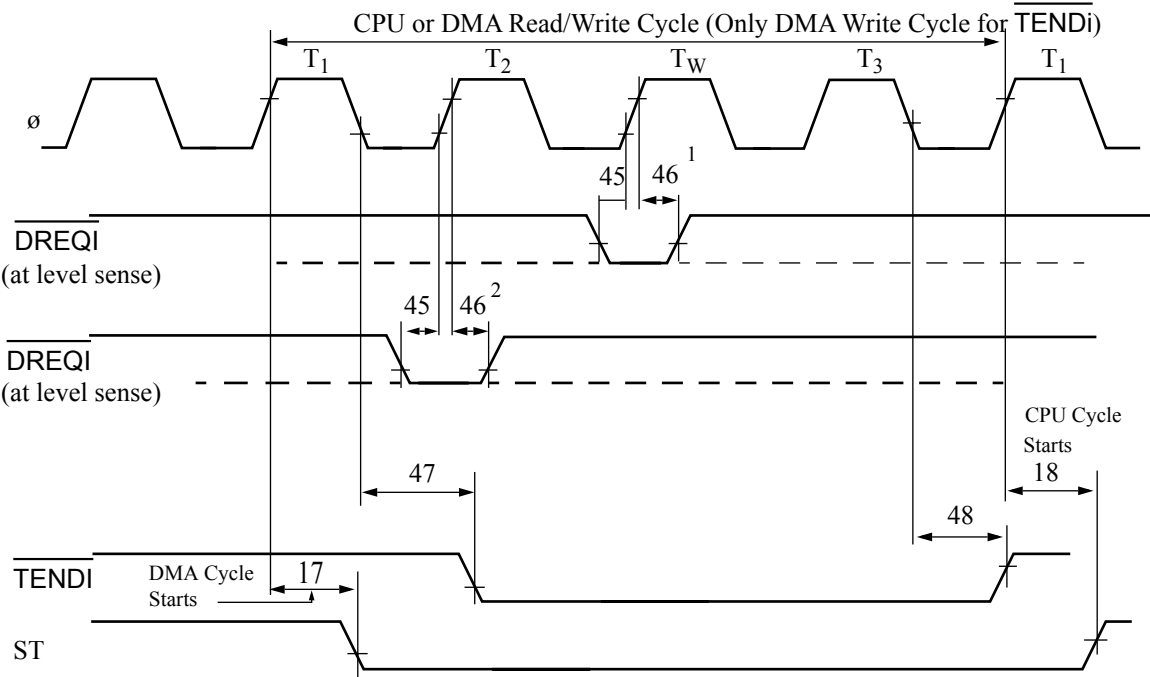


Figure 23. DMA Control Signals

$T_{\text{DRQS}}$  and  $T_{\text{DHQH}}$  are specified for the rising edge of clock followed by  $T_3$ .  $T_{\text{DRQS}}$  and  $T_{\text{DHQH}}$  are specified for the rising edge of clock.

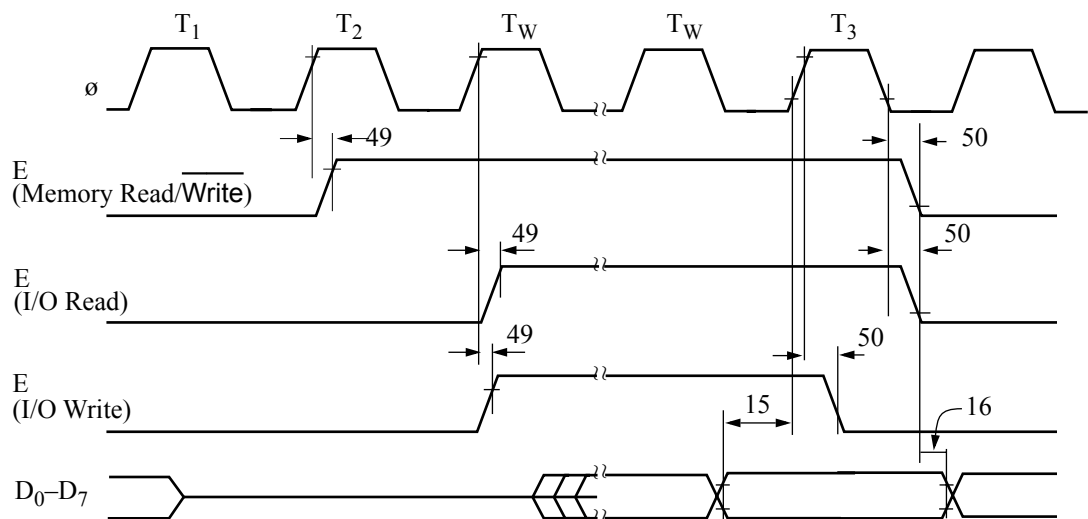


Figure 24. E Clock Timing  
(Memory Read/Write Cycle, I/O Read/Write Cycle)

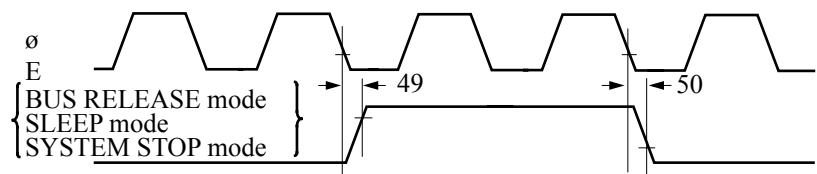


Figure 25. E Clock Timing  
(BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)

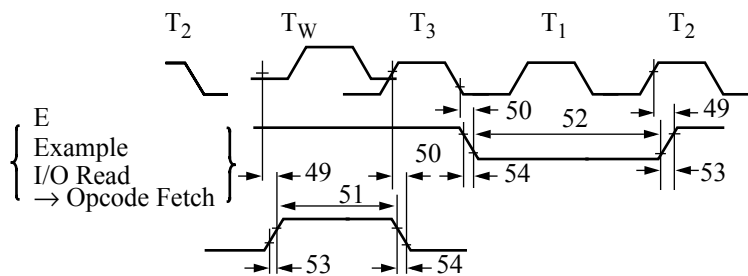
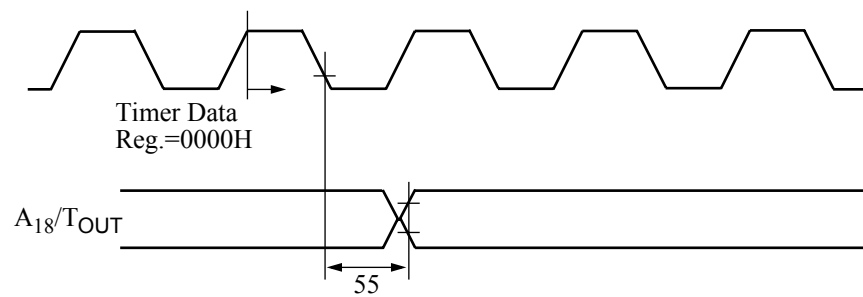
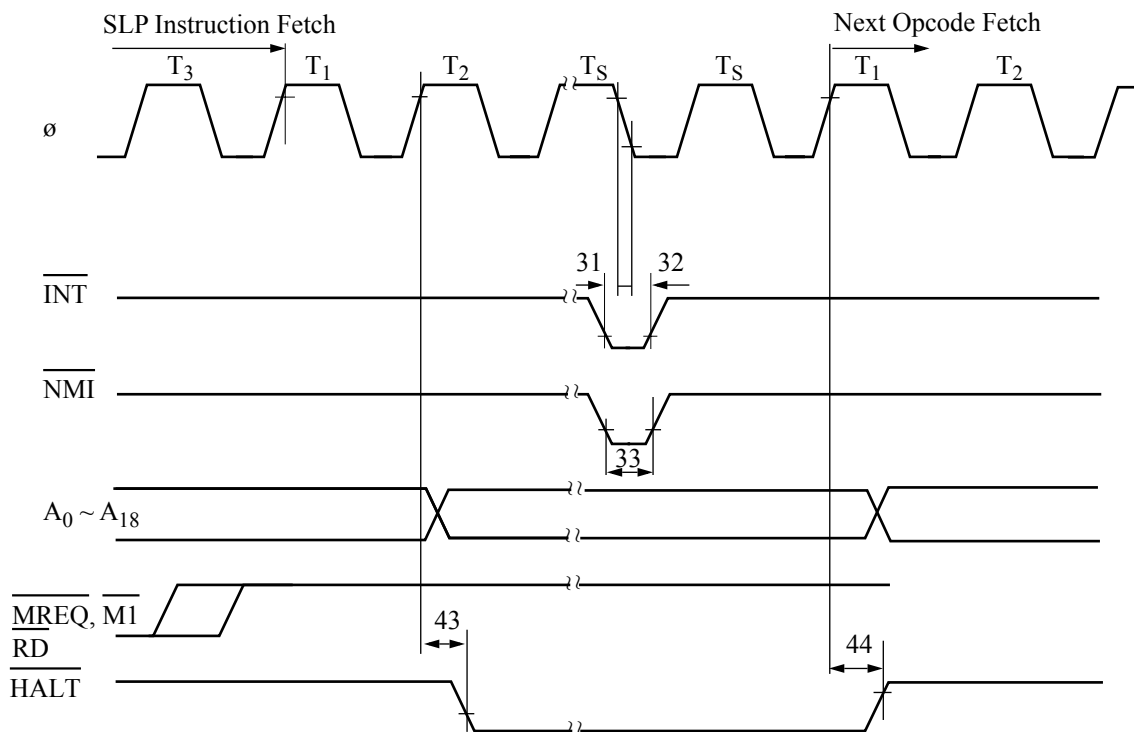


Figure 26. E Clock Timing  
(Minimum Timing Example of  $P_{WEL}$  and  $P_{WEH}$ )



**Figure 27. Timer Output Timing**



**Figure 28. SLP Execution Cycle**

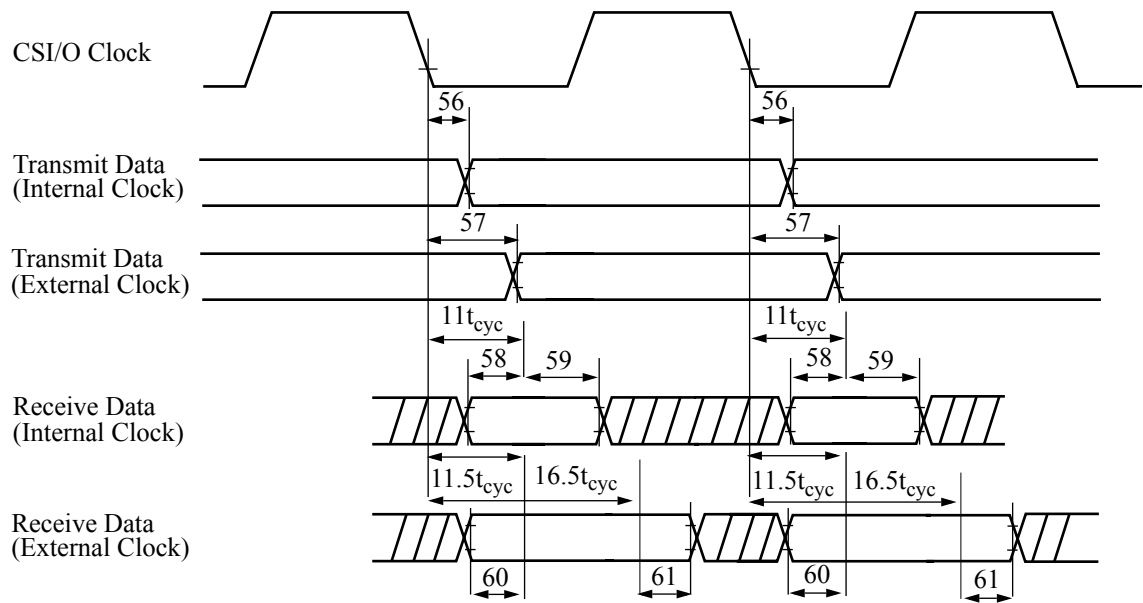


Figure 29. CSI/O Receive/Transmit Timing



Figure 30. Rise Time and Fall Times

CPU CONTROL REGISTER

**CPU Control Register (CCR).** This register controls the basic clock rate, certain aspects of Power-Down modes, and output drive/low noise options (Figure 31).

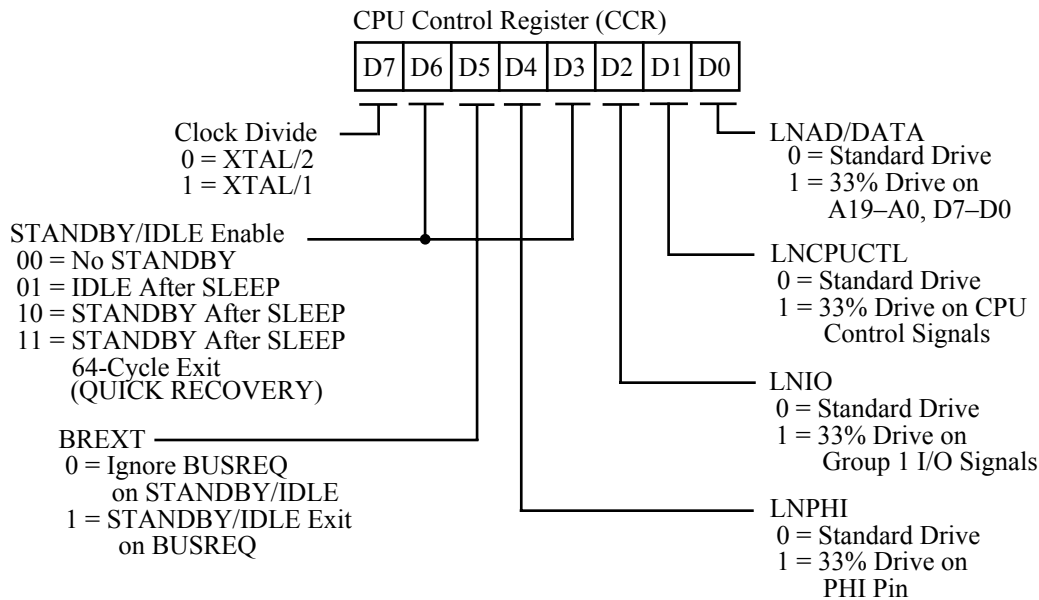


Figure 31. CPU Control Register (CCR) Address 1FH

**Bit 7.** Clock Divide Select. If this bit is 0, as it is after a Reset, the Z8S180/Z8L180 divides the frequency on the XTAL pin(s) by two to obtain its Master clock PHI. If this bit is programmed as 1, the part uses the XTAL frequency as PHI without division.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement provided in the AC Characteristics must be satisfied.

**Bits 6 and 3.** STANDBY/IDLE Control. When these bits are both 0, a SLP instruction makes the Z8S180/Z8L180 enter SLEEP or SYSTEM STOP mode, depending on the IOSTOP bit (ICR5).

When D6 is 0 and D3 is 1, setting the IOSTOP bit (ICR5) and executing a SLP instruction puts the Z8S180/Z8L180 into IDLE mode in which the on-chip oscillator runs, but its output is blocked from the rest of the part, including PHI out.

When D6 is 1 and D3 is 0, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into STANDBY mode, in which the on-chip oscillator is stopped and the part allows 217 (128K) clock cycles for the oscillator to stabilize when it restarts.

When D6 and D3 are both 1, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into QUICK RECOVERY STANDBY mode, in which the on-chip oscillator is stopped, and the part allows only 64 clock cycles for the oscillator to stabilize when it restarts.

The latter section, HALT and LOW POWER Modes, describes the subject more fully.

**Bit 5 BREXT.** This bit controls the ability of the Z8S180/Z8L180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

**Bit 4 LNPHI.** This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 33 percent of its drive capability.

**Bit 2 LNIO.** This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33percent of the original drive capability:

- $\overline{\text{RTSO/TxS}}$
- CKA1
- CKAO
- TXAO
- TXAI
- T<sub>OUT</sub>

**Bit 1 LNCPUCTL.** This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33percent the original drive capability:

- $\overline{\text{BUSACK}}$
- $\overline{\text{RD}}$
- $\overline{\text{WR}}$
- $\overline{\text{M1}}$
- $\overline{\text{MREQ}}$
- $\overline{\text{IORQ}}$
- $\overline{\text{RFSH}}$
- $\overline{\text{HALT}}$

**Bit 0 LNAD/DATA.** This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus output is reduced to 33 percent of its original drive capability.

ASCII REGISTER DESCRIPTION

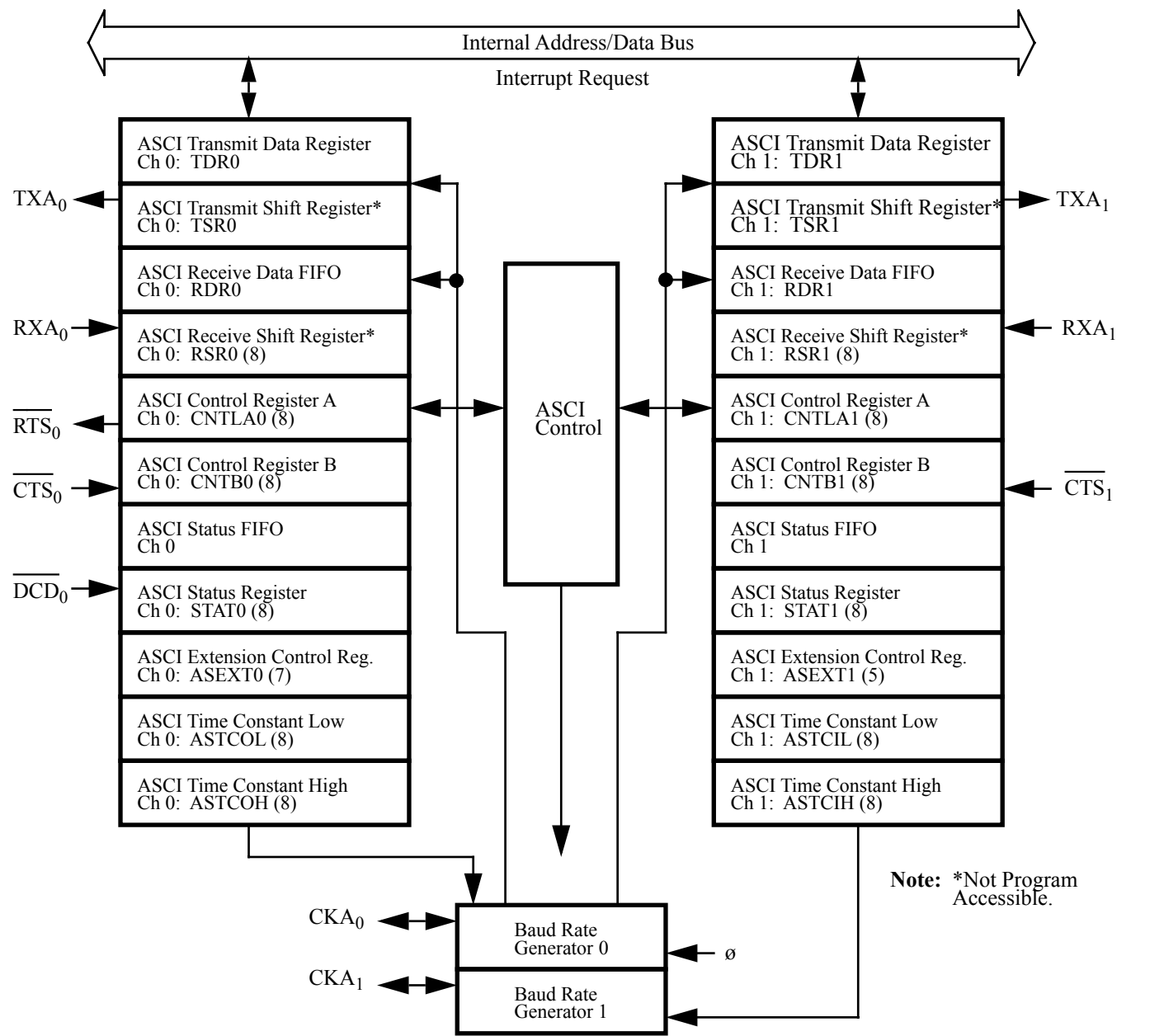


Figure 32. ASCII Block Diagram

**ASCII Transmit Register 0.** When the ASCII Transmit Register receives data from the ASCII Transmit Data Register (TDR), the data is shifted out to the TxA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR IDLEs by outputting a continuous High level. This register is not program accessible

**ASCII Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H).** Data written to the ASCII Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCII transmitter is double buffered.

Data can be written into and read from the ASCII Transmit Data Register. If data is read from the ASCII Transmit Data Register, the ASCII data transmit operation will not be affected by this read operation



**ASCII Receive Shift Register 0,1 (RSR0,1).** This register receives data shifted in on the RxA pin. When full, data is automatically transferred to the ASCII Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

ASCII Receive Data FIFO 0,1 (RDR0, 1: I/O Address = 08H, 09H). The ASCII Receive Data Register is a read-only

register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCII receiver is well buffered.

## ASCII STATUS FIFO

This four-entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest

character (if any) can be read from the ASCII status registers. A description follows.

## ASCII CHANNEL CONTROL REGISTER A

ASCII Control Register A 0 (CNTLA0: I/O Address = 00H)								
Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	$\overline{\text{RTS0}}$	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASCII Control Register A 1 (CNTLA1: I/O Address = 01H)								
Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	CKA1D	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 33. ASCII Channel Control Register A

**MPE: Multi-Processor Mode Enable (Bit 7).** The ASCII has a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the “wake-up” feature as follows. If MBE is set to 1, only received bytes in which the MPB (multiprocessor bit) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are “ignored” by the ASCII. If MPE is reset to 0, all bytes, regardless of the state of the MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

**RE: Receiver Enable (Bit 6).** When RE is set to 1, the ASCII transmitter is enabled. When TE is reset to 0, the

transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

**TE: Transmitter Enable (Bit 5).** When TE is set to 1, the ASCII receiver is enabled. When TE is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

**RTS0: Request to Send Channel 0 (Bit 4 in CNTLA0 Only).** If bit 4 of the System Configuration Register is 0, the RTS0/TxS pin has the RTS0 function. RTS0 allows the ASCII to control (start/stop) another communication devices transmission (for example, by connecting to that device’s CTS input). RTS0 is essentially

a 1 bit output port, having no side effects on other ASCII registers or flags.

Bit 4 in CNTLA1 is used.

$$\text{CKA1D} = 1, \overline{\text{CKA1/TEND0}} \text{ pin} = \overline{\text{TEND0}}$$
$$\text{CKA1D} = 0, \overline{\text{CKA1/TEND0}} \text{ pin} = \text{CKA1}$$

**MOD2, 1, 0: ASCII Data Format Mode 2, 1, 0 (bits 2-0).** These bits program the ASCII data format as follows.

**MOD2**

- =0→7 bit data
- =1→8 bit data

**MOD1**

- = 0→No parity
- = 1→Parity enabled

**MOD0**

- = 0→1 stop bit
- = 1→2 stop bits

Cleared to 0 on reset.

**MPBR/EFR: Multiprocessor Bit Receive/Error Flag Reset (Bit 3).** When multiprocessor mode is enabled (MP in CNTLB = 1), MPBR, when read, contains the value of the MPB bit for the most recent receive operation. When written to 0, the EFR function is selected to reset all error flags (OVRN, FE, PE and BRK in the ASEXT Register) to 0. MPBR/EFR is undefined during RESET.

The data formats available based on all combinations of MOD2, MOD1, and MOD0 are indicated in Table 5-6.

Table 5. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit data + 2 stop
0	1	0	Start + 7 bit data + parity + 1 stop
0	1	1	Start + 7 bit data + parity + 2 stop
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity + 1 stop
1	1	1	Start + 8 bit data + parity + 2 stop

ASCII CHANNEL CONTROL REGISTER B

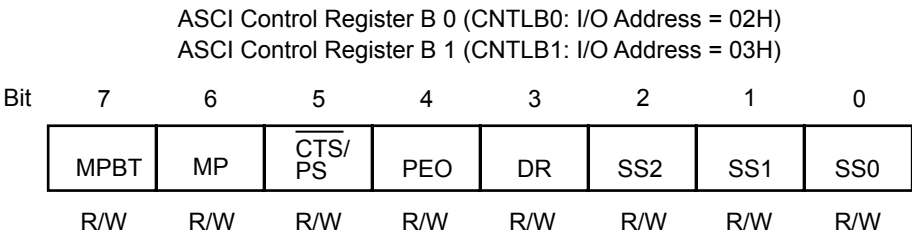


Figure 34. ASCII Channel Control Register B

**MPBT: Multiprocessor Bit Transmit (Bit 7).** When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If

MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

**MP: Multiprocessor Mode (Bit 6).** When MP is set to 1, the data format is configured for multiprocessor mode

based on MOD2 (number of data bits) and MOD0 (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP=1) format has no provision for parity. If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

**CTS/PS: Clear to Send/Prescale (Bit 5).** When read, CTS/PS reflects the state of the external CTS input. If the CTS input pin is HIGH, CTS/PS will be read as 1. Note that when the CTS input pin is HIGH, the TDRE bit is inhibited (that is, held at 0). For channel 1, the CTS input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, CTS/PS is only valid when read if the channel 1 CTS1E bit = 1 and the CTS input pin function is selected. The read data of CTS/PS is not affected by RESET.

If the SS2-0 bits in this register are not 111, and the BRG mode bit in the ASEX register is 0, then writing to this bit sets the prescale (PS) control as described in the following “Clock Modes” section. Under those circumstances, a 0 indicates a divide by 10 prescale function while a 1 indicates divide by 30. The bit resets to 0.

**PEO: Parity Even Odd (Bit 4)** . PEO selects even or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

**DR: Divide Ratio (Bit 3).** If the X1 bit in the ASEX register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

### SS2,1,0: Source/Speed Select 2,1,0 (Bits 2-0).

First, if these bits are 111, as they are after a Reset, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEX register.

If these bits are not 111 and the BRG mode bit is ASEX is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 9.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS has the CKAO function when bit 4 of the System Configuration Register is 0. DCD0/CKA1 has the CKA1 function when bit 0 of the Interrupt Edge register is 1.

Table 6. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

## ASCII STATUS REGISTER 0, 1 (STAT0, 1)

Each channel status register allows interrogation of ASCII communication, error and modem control signal status, and enabling or disabling of ASCII interrupts.

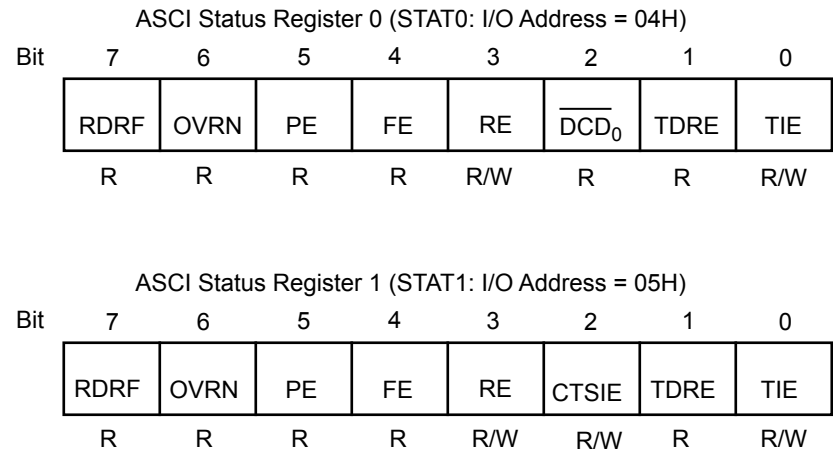


Figure 35. ASCII Status Registers

**RDRF: Receive Data Register Full (Bit 7).** RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and most recently received character in the FIFO from IOSTOP mode, during RESET and for ASCII0 if the DCD0 input is auto-enabled and is negated (High).

**OVRN: Overrun Error (Bit 6).** An overrun condition occurs if the receiver has finished assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register. The bit may also be cleared by RESET in IOSTOP mode or ASCII0 if the DCD0 pin is auto enabled and is negated (High).

**Note:** When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the most recent good character has come to the top of the FIFO so that OVRN is set. Software then writes a 1 to EFR to clear it.

**PE: Parity Error (Bit 5).** A parity error is detected when parity checking is enabled by the MOD1 bit in the CNT1LA register being 1, and a character has been assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until/unless the error character becomes the oldest one in the RxFIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register. This bit is also cleared by RESET in IOSTOP mode or ASCII0 if the DCD0 pin is auto-enabled and is negated (High).

**FE: Framing Error (Bit 4).** A framing error is detected when the stop bit of a character is sampled as 0/Space. However, this status bit is not set until/unless the error character becomes the oldest one in the RxFIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register. This bit is also cleared by RESET in IOSTOP mode or ASCII0 if the DCD0 pin is auto-enabled and is negated (High).

**REI: Receive Interrupt Enable (Bit 3).** RIE should be set to 1 to enable ASCII receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel requires its Request-routing field to be set to receive data from this ASCII. That is, if SM1-0 are 11 and SAR17-16 are 10, or DIM1 is 1 and IAR17-16 are 10, then ASCII1 does not request an interrupt for RDRF. If RIE is 1, either ASCII requests an interrupt when OVRN, PE or FE is set, and ASCII0 requests an interrupt when DCD0 goes High. RIE is cleared to 0 by Reset.

**DCD0: Data Carrier Detect (Bit 2 STAT0).** This bit is set to 1 when the pin is High. It is cleared to 0 on the first read of STAT0 following the pin's transition from High to Low and during RESET. Bit 6 of the ASEXT0 register is 0 to select auto-enabling, and the pin is negated (High). Channel 1 has an external CTS1 input which is multiplexed with the receive data pin RSX for the CSI/O.

Bit 2 = 0; Select RXS function.

Bit 2 = 1; Select CTS1 function.

**TDRE: Transmit Data Register Empty (Bit 1).** TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCIO, if the CTS0 pin is auto-enabled in the ASEXT0 registers and the pin is High, TDRE is reset to 0.

**TIE: Transmit Interrupt Enable (Bit 0).** TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt will be requested when TDRE = 1. TIE is cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

ASCI Transmit Data Registers  
Channel 0

Mnemonic TDR0

Address 06H

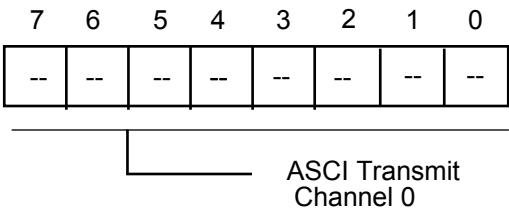


Figure 36. ASCII Register

ASCI Transmit Data Registers  
Channel 1

Mnemonic TDR1

Address 07H

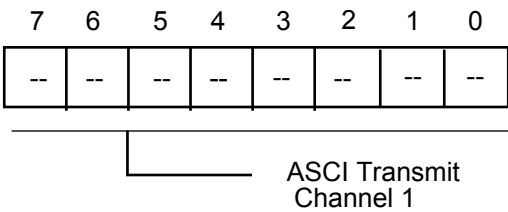


Figure 37. ASCII Register

ASCII RECEIVE REGISTER

Register addresses 08H and 09H hold the ASCII receive data for channel 0 and channel 1, respectively.

ASCII Receive Register Channel 0

Mnemonic TSR0

Address 08H



Figure 38. ASCII Receive Register Channel 0

ASCII Receive Register Channel 1

Mnemonic TSR1

Address 09H

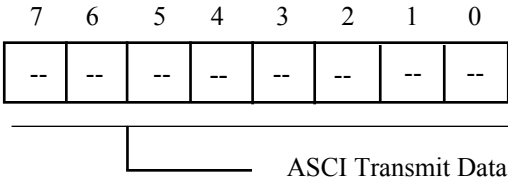


Figure 39. ASCII Receive Register Channel 1R

CSI/O CONTROL/STATUS REGISTER

CNTR is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.

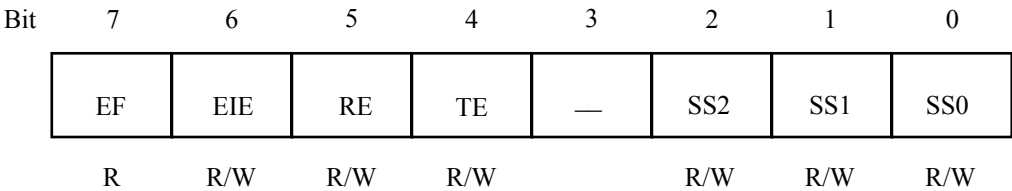


Figure 40. CSI/O Control Register

- EF: End Flag (Bit 7).** EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If EIE (End Interrupt Enable) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF = 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.
- EIE: End Interrupt Enable (Bit 6).** EIE is set to 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.
- RE: Receive Enable (Bit 5).** A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the

- data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted in on the RXS pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are never both set to 1 at the same time. RE is cleared to 0 during RESET and IOSTOP mode.
- Transmit Enable (bit 4).** A CSI/O transmit operation is started by setting TE to 1. When TE is set to 1, the data clock is enabled. When in internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted out

on the TXS pin synchronous with the (internal or external) data clock. After transmitting 8 bits of data, the CSI/O automatically clears TE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. TE and RE are never both set to 1 at the same time. TE is cleared to 0 during RESET and IOSTOP mode.

**SS2, 1, 0: Speed Select 2, 1, 0 (bits 2-0).** SS2, SS1 and SS0 select the CSI/O transmit/receive clock source and speed. SS2, SS1 and SS0 are all set to 1 during RESET. Table 10 indicates CSI/O Baud Rate Selection.

Table 7. CSI/O Baud Rate Selection

SS2	SS1	SS0	Divide Ratio
0	0	0	÷20
0	0	1	÷40
0	1	0	÷80
0	1	1	÷160
1	0	0	÷320
1	0	1	÷640
1	1	0	÷1280
1	1	1	External Clock Input (Less Than ÷20.)

After RESET, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

## CSI/O Transmit/Receive Data Register

Mnemonic TRDR  
Address 0BH.

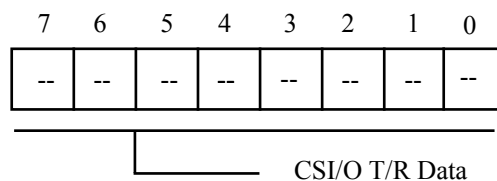


Figure 41. CSI/O Transmit/Receive Data Register 1R

## Timer Data Register Channel 0L

Mnemonic TMDR0L  
Address 0CH

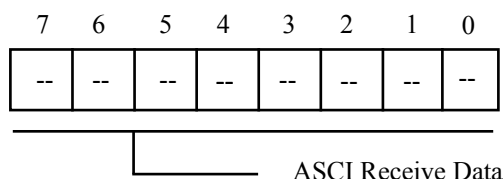


Figure 42. Timer Register Channel 0L

## Timer Data Register Channel 0H

Mnemonic TMDR0H  
Address 0DH

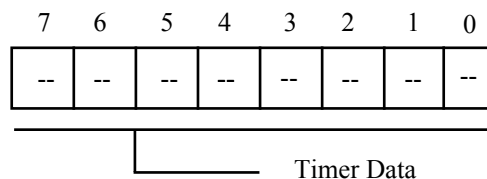


Figure 43. Timer Data Register Channel 0H

## Timer Reload Register 0L

Mnemonic RLDR0L  
Address 0EH

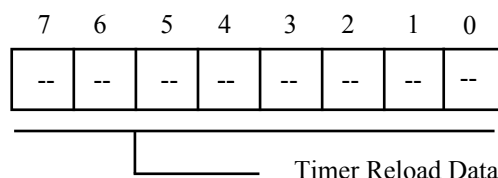


Figure 44. Timer Reload Register Low

Timer Reload Register 0H

Mnemonic RLDR0H  
Address 0FH

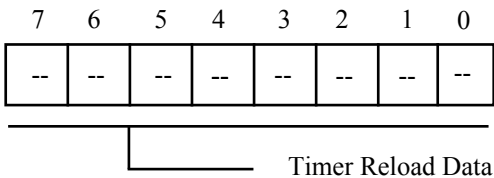


Figure 45. Timer Reload Register Channel

TIMER CONTROL REGISTER (TCR)

TCR monitors both channels (PRT0, PRT1) TMDR status. It also controls enabling and disabling of down counting and interrupts along with controlling output pin A18/T<sub>OUT</sub> for PRT1.

Bit	7	6	5	4	3	2	1	0
	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Figure 46. Timer Control Register (TCR: I/O Address = 10H)

**TIF1: Timer Interrupt Flag 1 (Bit 7)** . When TMDR1 decrements to 0, TIF1 is set to 1. This condition generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

**TIF0: Timer Interrupt Flag 0 (Bit 6).** When TMDR0 decrements to 0, TIF0 is set to 1. This generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

**TIE1: Timer Interrupt Enable 1 (Bit 5).** When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

**TOC1, 0: Timer Output Control (Bits 3, 2).** TOC1 and TOC0 control the output of PRT1 using the multiplexed T<sub>OUT</sub>/DREQ pin as indicated in Table 11. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the T<sub>OUT</sub> function is selected. By programming TOC1 and TOC0, the T<sub>OUT</sub>/DREQ pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

Table 8. Timer Output Control			
TOC1	TOC0	Output	
0	0	Inhibited	The T <sub>OUT</sub> /DREQ pin is not affected by the PRT.
0	1	Toggled	If bit 3 of IAR1B is 1, the T <sub>OUT</sub> /DREQ pin is toggles or set Low or High as indicated.
1	0	0	
1	1	1	

**TDE1, 0: Timer Down Count Enable (Bits 1, 0).** TDE1 and TDE0 enable and disable down counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0, 1) is set to 1, down counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.



## ASCI EXTENSION CONTROL REGISTER CHANNEL 0 (ASEXT0) AND CHANNEL 1 (ASEXT1)

**Notes:** The Extension Control Register controls functions that have been added to the ASCIs in the Z8S180/Z8L180 family. All bits in this register reset to 0.

ASCI Extension Control Register 0 (ASEXT0 I/O Address = 12H)							
Bit	7	6	5	4	3	2	1 0
	Reserved	DCDO	CTSO	XI	BRGO Mode	Break Nab	Break Send Break

ASCI Extension Control Register 1 (ASEXT1 I/O Address = 13H)							
Bit	7	6	5	4	3	2	1 0
	Reserved	Reserved	Reserved	XI	BRGI Mode	Break Enab	Break Send Break

Figure 47. ASCI Extension Control Registers, Channel 0 and 1

**DCDO (Bit 6, ASCI0 Only).** If this bit is 0, then the DCD0 pin auto-enables the ASCI0 receiver, such that when the pin is negated/High, the Receiver is held in a RESET state. The state of the DCD-pin has no effect on receiver operation. In either state of this bit, software can read the state of the DCD0 pin in the STAT0 register, and the receiver will interrupt on a rising edge of DCD0.

**CTSO (Bit 5, ASCI0 Only).** If this bit is 0, then the CTS0 pin auto-enables the ASCI0 transmitter, in that when the pin is negated/high, the TDRE bit in the STAT0 register is forced to 0. If this bit is 1, the state of the CTS0 pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the CTS0 pin the CNTLB0 register.

**X1 (Bit 4).** If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a 1X bit clock (sometimes called Isochronous mode). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RxA pin is not required to be synchronized to a clock.

**BRG Mode (Bit 3).** If the SS2-0 bits in the CNTLB register are not 111, and this bit is 0, the ASCI's Baud Rate Generator divides PHI by 10 or 30, depending on the DR bit in CNTLB, and then by a power of two selected by the SS2-0 bits, to obtain the clock that is presented to the transmitter and receiver and that can be output on the CKA pin. If SS2-0 are not 111, and this bit is 1, the Baud Rate Generator

divides PHI by twice (the 16-bit value programmed into the Time Constant Registers, plus two). This mode is identical to the operation of the baud rate generator in the ESCC.

**Break Enable (Bit 2).** If this bit is 1, the receiver will detect Break conditions and report them in bit 1, and the transmitter will send Breaks under the control of bit 0.

**Break Detect (Bit 1).** The receiver sets this read-only bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the Rx FIFO. The bit is cleared when software writes a 0 to the EFR bit in CNTLA register, also by RESET, by IOSTOP mode, and for ASCIO if the DCD0 pin is auto-enabled and is negated (High).

**Send Break (Bit 0).** If this bit and bit 2 are both 1, the transmitter holds the TXA pin low to send a Break condition. The duration of the Break is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

### Timer Data Register Channel 1L

Mnemonic TMDR1L  
Address 14H

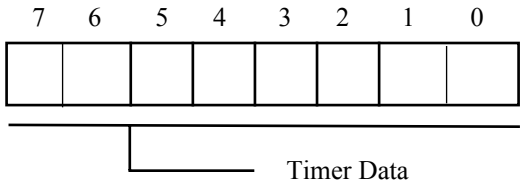


Figure 48. Timer Data Register 1L

### Timer Data Register Channel 1H

Mnemonic TMDR1H  
Address 15H

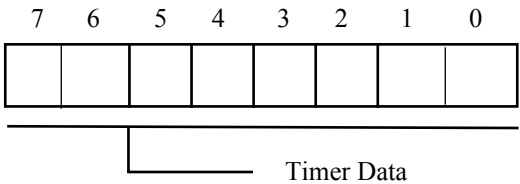


Figure 49. Timer Data Register 1H

### Timer Reload Register Channel 1L

Mnemonic RLDR1L  
Address 16

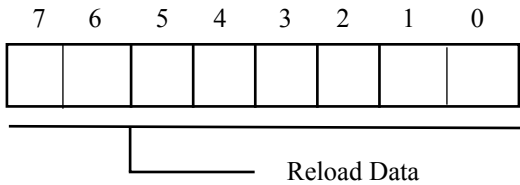


Figure 50. Timer Reload Channel 1L

### Timer Reload Register Channel 1H

Mnemonic RLDR1H  
Address 17H

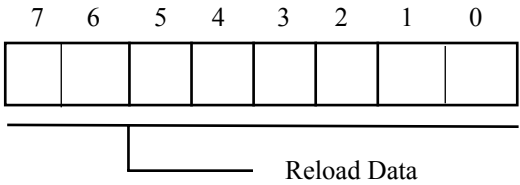


Figure 51. Timer Reload Register Channel 1H

### Free Running Counter (Read Only)

Mnemonic FRC  
Address 18H

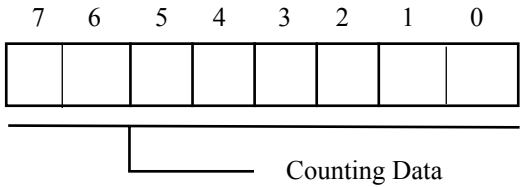


Figure 52. Free Running Counter

ASCI TIME CONSTANT REGISTERS

If the SS2-0 bits of the CNTLA register are not 111, and the BRG Mode bit in the ASEXT register is 1, the ASCI divides the PHI clock by twice (the 16-bit value in these registers, plus two), to obtain the clock that is presented to the transmitter and receiver for division by 1, 16, or 64 and that can be output on the CKA1 pin.

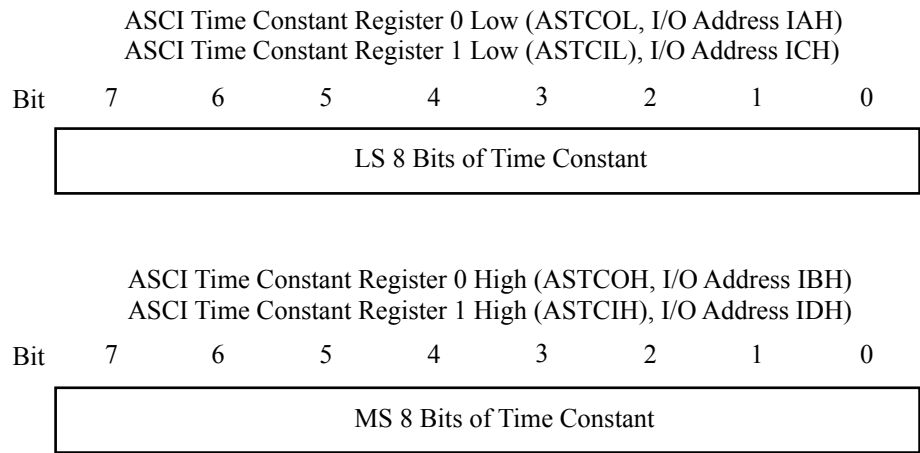


Figure 53. ASCI Time Constant Registers

CLOCK MULTIPLIER REGISTER

(Z180 MPU Address 1EH)

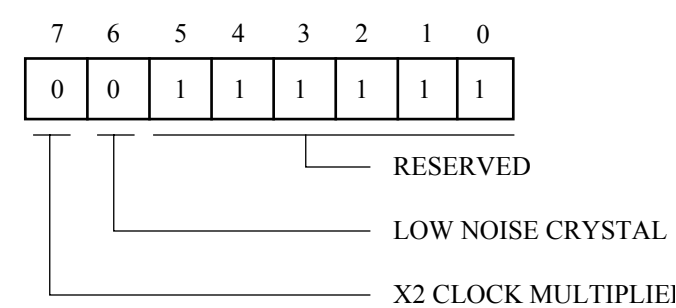


Figure 54. Clock Multiplier Register

**Bit 7. X2 Clock Multiplier Mode.** When this bit is set to 1, the programmer can double the internal clock from that of the external clock. This feature only operates effectively with frequencies of 10–16 MHz (20–32 MHz internal). When this bit is set to 0, the Z8S180/Z8L180 device operates in normal mode. At power-up, this feature is disabled.

**Bit 6. Low Noise Crystal Option.** Setting this bit to 1 enables the low noise option for the EXTAL and XTAL pins. This option reduces the gain in addition to reducing the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications, where the crystal may be driven too hard by the oscillator. Setting this bit to 0 is selected for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

**Note:** Operating restrictions for device operation are listed below. If a low noise option is required, and normal device operation is required, use the clock multiplier feature.

Low Noise ADDR 1E, bit 6=1	Normal ADDR 1E, bit 6=0
20 MHz @ 4.5V, 100°C	33 MHz @ 4.5V, 100°C
10 MHz @ 3.0V, 100°C	20 MHz @ 3.0V, 100°C

Table 9. Low Noise Option

DMA SOURCE ADDRESS REGISTER CHANNEL 0

The DMA Source Address Register Channel 0 specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64 KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal.

DMA Source Address Register, Channel 0L

Mnemonic SAR0L

Address 20H



Figure 55. DMA Source Address Register 0L

DMA Source Address Register, Channel 0H

Mnemonic SAR0H

Address 21H



Figure 56. DMA Source Address Register 0H

DMA Source Address Register Channel 0B

Mnemonic SAR0B

Address 22H



Figure 57. DMA Source Address Register 0B

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64 KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0L

Mnemonic DAR0L

Address 23H



Figure 58. DMA Destination Address Register Channel 0L

DMA Destination Address Register Channel 0H

Mnemonic DAR0H

Address 24H



Figure 59. DMA Destination Address Register Channel 0H

DMA Destination Address Register Channel 0B

Mnemonic DAR0B

Address 25H



Figure 60. DMA Destination Address Register Channel 0B

**Note:** In the R1 and Z Mask, these DMA registers are expanded from 4 bit to 3 bits in the package version of CP-68

				DMA Transfer Request
A19	A18	A17	A16	
X	X	0	0	DREQ0
X	X	0	1	TDR0 (ASCI0)
X	X	1	0	TDR1 (ASCI1)
X	X	1	1	Not Used

DMA BYTE COUNT REGISTER CHANNEL 0

The DMA Byte Count Register Channel 0 specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64 KB transfers. When one byte is transferred, the register is decremented by one. If “n” bytes should be transferred, “n” must be stored before the DMA operation.

**Note:** All DMA Count Register channels are undefined during RESET.

DMA Byte Count Register Channel 0L

Mnemonic BCR0L  
Address 26H

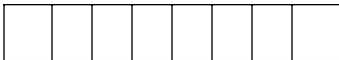


Figure 61. DMA Byte Count Register 0L

DMA Byte Count Register Channel 0H

Mnemonic BCR0H  
Address 27H

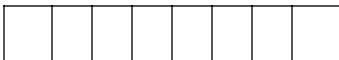


Figure 62. DMA Byte Count Register 0H

DMA Byte Count Register Channel 1L

Mnemonic BCR1L  
Address 2EH

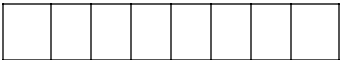


Figure 63. DMA Byte Count Register 1L

DMA Byte Count Register Channel 0H

Mnemonic BCR1H  
Address 2FH

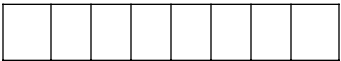


Figure 64. DMA Byte Count Register 0H

### DMA MEMORY ADDRESS REGISTER CHANNEL 1

The DMA Memory Address Register Channel 1 specifies the physical memory address for channel 1 transfers. The address may be a destination or a source memory location. The register contains 20 bits and may specify up to 1024 KB memory addresses.

#### DMA Memory Address Register, Channel 1L

Mnemonic MAR1L  
Address 28H

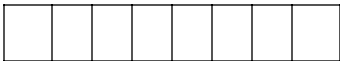


Figure 65. DMA Memory Address Register, Channel 1L

#### DMA Memory Address Register, Channel 1H

Mnemonic MAR1H  
Address 29H

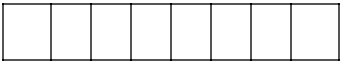


Figure 66. DMA Memory Address Register, Channel 1H

#### DMA Memory Address Register, Channel 1B

Mnemonic MAR1B  
Address 2AH



Figure 67. DMA Memory Address Register, Channel 1B

### IAR MS BYTE REGISTER

The IAR MS Byte Register specifies the I/O address for channel 1 transfers. This may be destination or source I/O address. The register contains 16 bits. The most significant

byte identifies the Request Handshake signal and controls the Alternating Channel feature.  
All bits in IAR1B reset to 0.

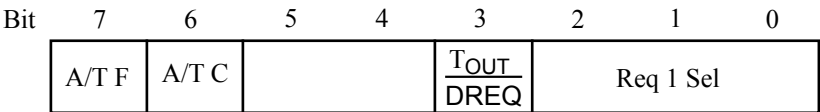


Figure 68. IAR MS Byte Register (IAR1B: I/O Address 2DH)



DMA I/O Address Register Channel 1L

Mnemonic IAR1L

Address 2BH

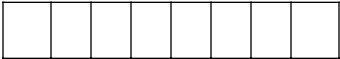


Figure 69. DMA I/O Address Register Channel 1L

DMA I/O Address Register Channel 1H

Mnemonic IAR1H

Address 2CH

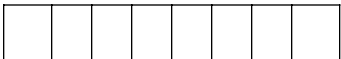


Figure 70. DMA I/O Address Register Channel 1H

DMA I/O Address Register Channel 1B

Mnemonic IAR1B

Address 2DH



Figure 71. DMA I/O Address Register Channel 1B

DMA STATUS REGISTER (DSTAT)

DSTAT is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also indicates DMA transfer status, Completed or In Progress.

DMA Status Register

Mnemonic DSTAT  
Address 30

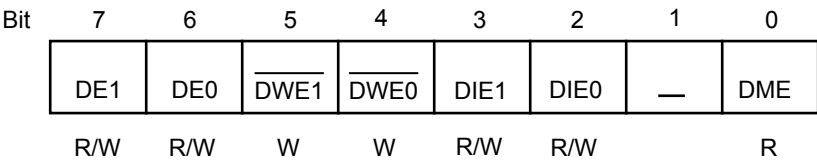


Figure 72. DMA Status Register (DSTAT: I/O Address = 30H)

**DE1: DMA Enable Channel 1 (Bit 7).** When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software write to DE1, DWE1 should be written with 0 during the same register write access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DME (DMA Main Enable) to 1. DE1 is cleared to 0 during RESET.

**DE0: DMA Enable Channel 0 (Bit 6).** When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software write to DE0, DWE0 should be written with 0 during the same register write access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DME (DMA Main Enable) to 1. DE0 is cleared to 0 during RESET.

**DWE1: DE1 Bit Write Enable (Bit 5).** When performing any software write to DE1, DWE1 should be written with 0 during the same access. DWE1 always reads as 1.

**DWE0: DE0 Bit Write Enable (Bit 4).** When performing any software write to DE0, DWE0 should be written with 0 during the same access. DWE0 always reads as 1.

**DIE1: DMA Interrupt Enable Channel 1 (Bit 3).** When DIE0 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 = 0) causes a CPU interrupt

request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

**DIE0: DMA Interrupt Enable Channel 0 (Bit 2).** When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

**DME: DMA Main Enable (Bit 0).** A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When NMI occurs, DME is reset to 0, thus disabling DMA activity during the NMI interrupt service routine. To restart DMA, DE— and/or DE1 should be written with 1 (even if the contents are already 1). This condition automatically sets DME to 1, allowing DMA operations to continue. Note that DME cannot be directly written. The bit is cleared to 0 by NMI or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

DMA MODE REGISTER (DMODE)

DMODE is used to set the addressing and transfer mode for channel 0.

DMA Status Register

Mnemonic DMODE

Address 31H

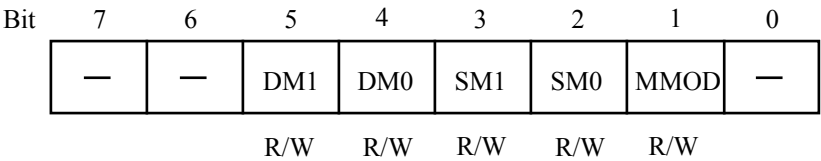


Figure 73. DMA Mode Register (DMODE: I/O Address = 31H)

**DM1, DM0: Destination Mode Channel 0 (Bits 5,4).** This mode specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET.

Table 10. Channel 0 Destination

DM1	DM0	Memory	
		Memory I/O	Increment/Decrement
0	0	Memory	+1
0	1	Memory	−1
1	0	Memory	fixed
1	1	I/O	fixed

**SM1, SM0: Source Mode Channel 0 (Bits 3, 2).** This mode specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred.

Table 11. Channel 0 Source

SM1	SM0	Memory	
		Memory I/O	Increment/Decrement
0	0	Memory	+1
0	1	Memory	−1
1	0	Memory	fixed
1	1	I/O	fixed

Table 12 indicates all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Since I/O to/from I/O transfers are not implemented, 12 combinations are available.

*Table 12. Transfer Mode Combinations)*

DM1	DM0	SM1	SM0	Transfer Mode	Address
					Increment/Decrement
0	0	0	0	Memory→Memory	SAR0+1, DAR0+1
0	0	0	1	Memory→Memory	SAR0−1, DAR0+1
0	0	1	0	Memory*→Memory	SAR0 fixed, DAR0+1
0	0	1	1	I/O→Memory	SAR0 fixed, DAR0+1
0	1	0	0	Memory→Memory	SAR0+1, DAR0−1
0	1	0	1	Memory→Memory	SAR0−1, DAR0−1
0	1	1	0	Memory*→Memory	SAR0 fixed, DAR0−1
0	1	1	1	I/O→Memory	SAR0 fixed, DAR0−1
1	0	0	0	Memory→Memory*	SAR0+1, DAR0 fixed
1	0	0	1	Memory→Memory*	SAR0−1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Memory→I/O	SAR0+1, DAR0 fixed
1	1	0	1	Memory I/O	SAR0−1, DAR0 fixed
1	1	1	0	Reserved	
1	1	1	0	Reserved	

**Note:** \* Includes memory mapped I/O.

**MMOD: Memory Mode Channel 0 (Bit 1).** When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC

takes control of the bus continuously until the DMA transfer completes (as indicated by the byte count register = 0). In cycle steal mode, the CPU is given a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected Request signal times the transfer ignoring MMOD. MMOD is cleared to 0 during RESET.

## DMA/WAIT CONTROL REGISTER (DCNTL)

DCNTL controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. Also, the register defines the Request signal for each channel as level or edge

sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.

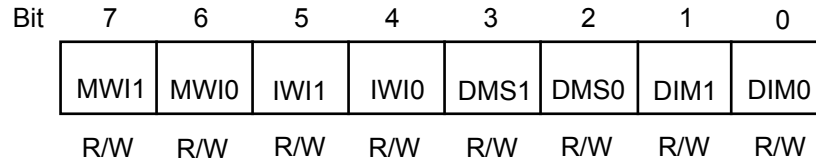


Figure 74. DMA/WAIT Control Register (DCNTL: I/O Address = 32H)

**MWI1, MWI0: Memory Wait Insertion (Bits 7-6).** This bit specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET.

MWI1	MWI0	Wait State
0	0	0
0	1	1
1	0	2
1	1	3

**IWI1, IWI0: I/O Wait Insertion (Bits 5-4).** This bit specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET. See the section on Wait-State Generation for details.

IWI1	IWI0	Wait State
0	0	0
0	1	2
1	0	3
1	1	4

**DMS1, DMS0: DMA Request Sense (Bits 3-2).** DMS1 and DMS0 specify the DMA request sense for channel 0 and channel 1 respectively. When reset to 0, the input is level sense. When set to 1, the input is edge sense. DMS1 and DMS0 are cleared to 0 during RESET.

DMSi	Sense
1	Edge Sense
0	Level Sense

Typically, for an input/source device, the associated DMS bit should be programmed as 0 for level sense because the device has a relatively long time to update its Request signal

after the DMA channel reads data from it in the first of the two machine cycles involved in transferring a byte.

An output/destination device has much less time to update its Request signal, after the DMA channel starts a write operation to it, as the second machine cycle of the two cycles involved in transferring a byte. With zero-wait state I/O cycles, a device cannot update its Request signal in the required time, so edge sensing must be used.

A one-wait-state I/O cycle also does not provide sufficient time for updating, so edge sensing is again required.

**DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (Bits 1-0).** Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. DIM1 and DIM0 are cleared to 0 during RESET.

Table 13. Channel 1 Transfer Mode

		Address	
DIM1	DIM0	Transfer Mode	Increment/Decrement
0	0	Memory→I/O	MAR1 +1, IAR1 fixed
0	1	Memory→I/O	MAR1-1, IAR1 fixed
1	0	I/O→Memory	IAR1 fixed, MAR1 + 1
1	1	I/O→Memory	IAR1 fixed, MAR1 -1

## INTERRUPT VECTOR LOW REGISTER

Bits 7-5 of IL are used as bits 7-5 of the synthesized interrupt vector during interrupts for the INT1 and INT2 pins and for the DMAs, ASCIs, PRTs, and CSI/O. These three bits are cleared to 0 during Reset (Figure 75).

### Interrupt Vector Low Register

Mnemonic: IL  
Address 33H

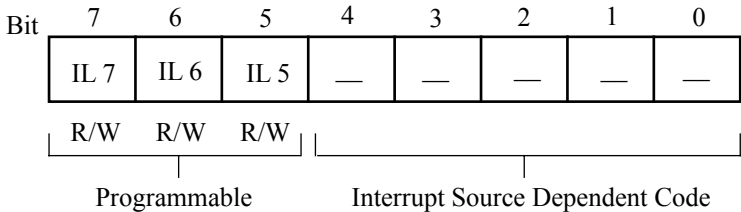


Figure 75. Interrupt Vector Low Register (IL: I/O Address = 33H)

## INT/TRAP CONTROL REGISTER

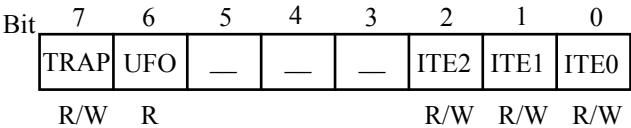
This register is used in handling TRAP interrupts and to enable or disable Maskable Interrupt Level 0 and the INT1 and INT2 pins.

### INT/TRAP Control Register

Mnemonics ITC  
Address 34H

- ESCC
- CTCs
- Bidirectional Centronics controller
- External interrupt input  $\overline{\text{INT0}}$

A 1 in a bit enables the corresponding interrupt level while a 0 disables it. A Reset sets ITE0 to 1 and clears ITE1 and ITE2 to 0.



**TRAP (Bit 7).** This bit is set to 1 when an undefined Opcode is fetched. TRAP can be reset under program control by writing it with a 0; however, it cannot be written with 1 under program control. TRAP is reset to 0 during RESET.

**UFO: Undefined Fetch Object (Bit 6).** When a TRAP interrupt occurs, the contents of UFO allow determination of the starting address of the undefined instruction. This interrupt is necessary because the TRAP may occur on either the second or third byte of the Opcode. UFO allows the stacked PC value to be correctly adjusted. If UFO = 0, the first Opcode should be interpreted as the stacked PC-1. If UFO = 1, the first Opcode address is stacked PC-2. UFO is Read-Only.

**ITE2, 1, 0: Interrupt Enable 2, 1, 0 (Bits 2-0).** ITE2 and ITE1 enable and disable the external interrupt inputs INT2 and INT1, respectively. ITE0 enables and disables interrupts from:

**TRAP Interrupt.** The Z8S180/Z8L180 generates a nonmaskable (not affected by the state of IEF1) TRAP interrupt when an undefined Opcode fetch occurs. This feature can be used to increase software reliability, implement an “extended” instruction set, or both. TRAP may occur during Opcode fetch cycles and also if an undefined Opcode is fetched during the interrupt acknowledge cycle for INT<sub>0</sub> when Mode 0 is used.

When a TRAP interrupt occurs, the Z8S180/Z8L180 operates as follows:

1. The TRAP bit in the Interrupt TRAP/Control (ITC) register is set to 1.
2. The current PC (Program Counter) value, reflecting the location of the undefined Opcode, is saved on the stack.
3. The Z8S180/Z8L180 vectors to logical address 0. Note that if logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC will reveal whether the restart at physical address 00000H was caused by RESET or TRAP.

All TRAP interrupts occur after fetching an undefined second Opcode byte following one of the prefix Opcodes (CBH, DDH, EDH, or FDH) or after fetching an undefined third Opcode byte following one of the double-prefix Opcodes (DDCBH or FDCBH).

The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly “adjust” the stacked PC, depending on whether the second or third byte of the Opcode generated the TRAP. If UFO=0, the starting address of the invalid instruction is equal to the stacked PC-1. If UFO=1, the starting address of the invalid instruction is equal to the stacked PC-2.

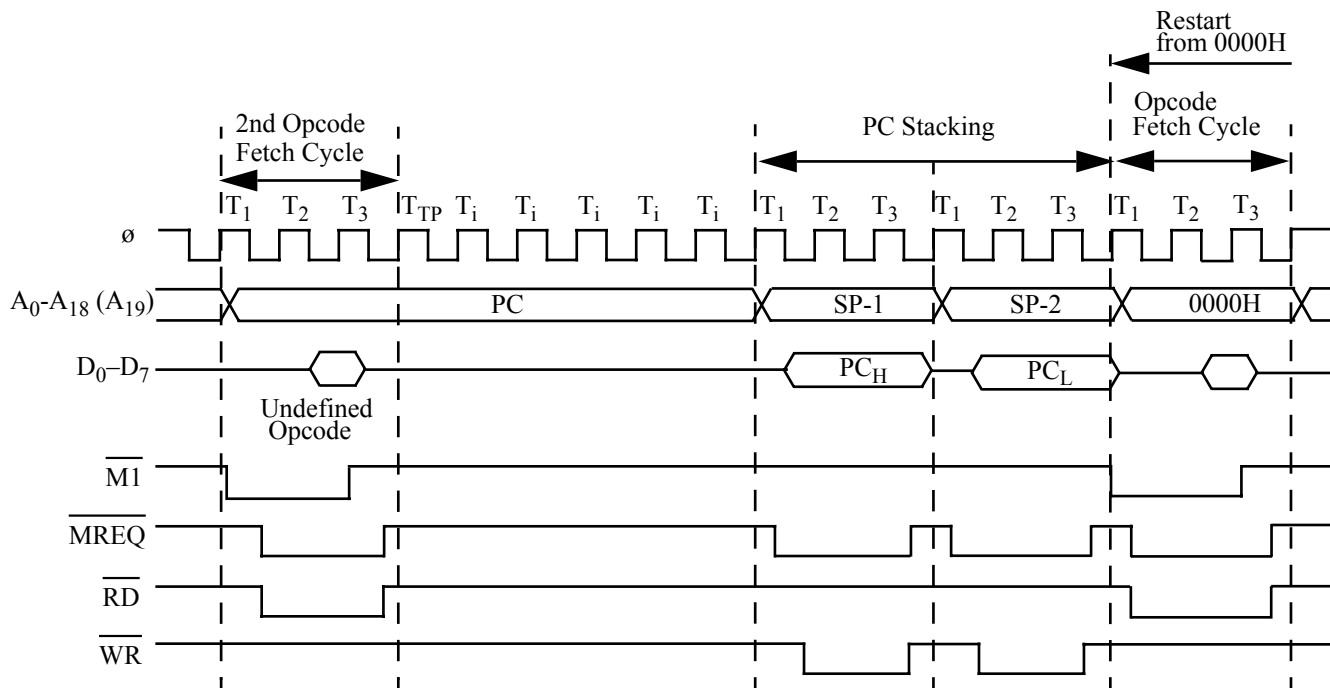


Figure 76. TRAP Timing-2<sup>nd</sup> Opcode Undefined

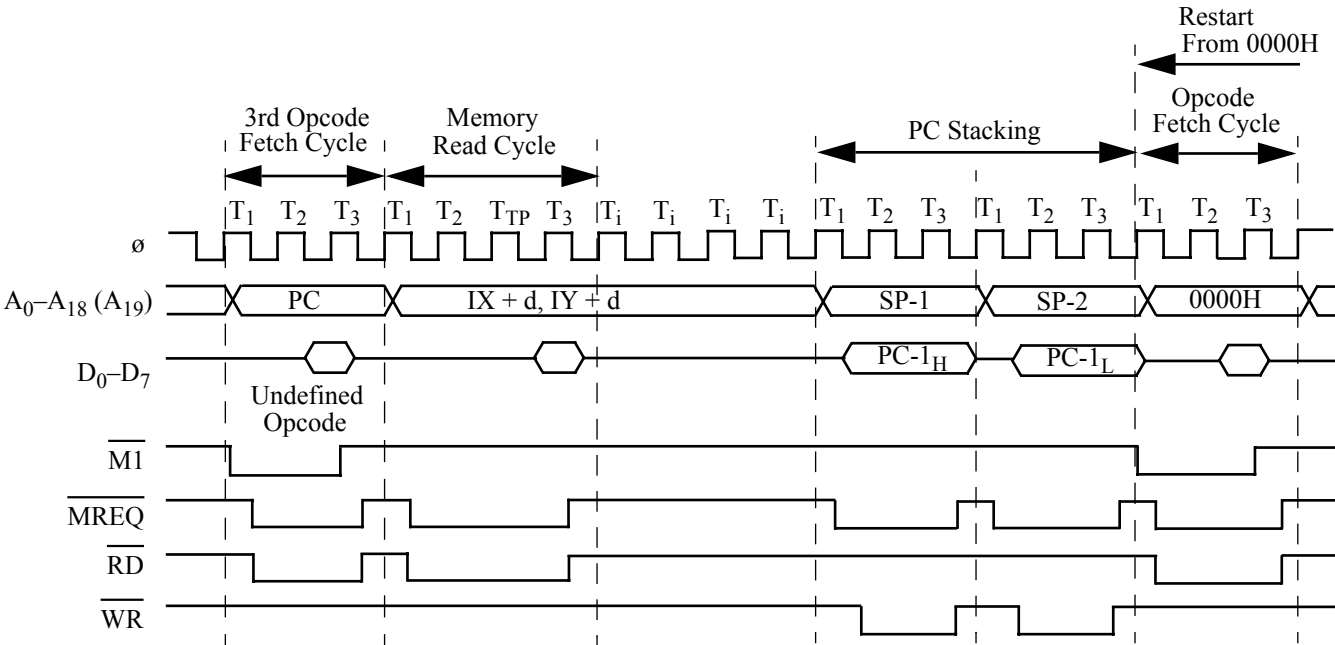


Figure 77. TRAP Timing—3<sup>rd</sup> Opcode Undefined

## REFRESH CONTROL REGISTER

Mnemonic RCR

Address 36H

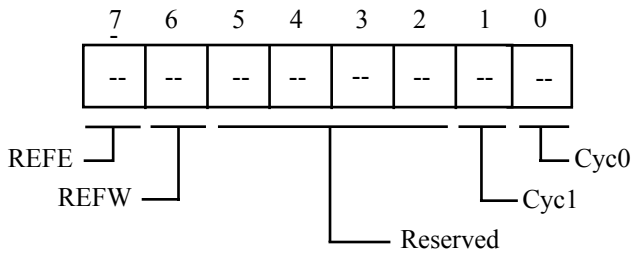


Figure 78. Refresh Control Register  
(RCA: I/O Address = 36H)

The RCR specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.



**Refe: Refresh Enable (Bit 7).** REFE = 0 disables the refresh controller while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

**REFW: Refresh Wait (Bit 6).** REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET.

**CYC1, 0: Cycle Interval (Bit 1,0).** CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. In the case of dynamic RAMs requiring 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625  $\mu$ s. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see Table 14).

Table 14. DRAM Refresh Intervals

CYC1	CYC0	Insertion	Time Interval				
		Interval	Ø: 10 MHz	8 MHz	6 MHz	4 MHz	2.5 MHz
0	0	10 states	(1.0 $\mu$ s)*	(1.25 $\mu$ s)*	1.66 $\mu$ s	2.5 $\mu$ s	4.0 $\mu$ s
0	1	20 states	(2.0 $\mu$ s)*	(2.5 $\mu$ s)*	3.3 $\mu$ s	5.0 $\mu$ s	8.0 $\mu$ s
1	0	40 states	(4.0 $\mu$ s)*	(5.0 $\mu$ s)*	6.6 $\mu$ s	10.0 $\mu$ s	16.0 $\mu$ s
1	1	80 states	(8.0 $\mu$ s)*	(10.0 $\mu$ s)*	13.3 $\mu$ s	20.0 $\mu$ s	32.0 $\mu$ s

**Note:** \*calculated interval

**Refresh Control and Reset.** After RESET, based on the initialized value of RCR, refresh cycles will occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

#### Dynamic RAM Refresh Operation

- Refresh Cycle insertion is stopped when the CPU is in the following states:
  - During RESET
  - When the bus is released in response to  $\overline{\text{BUSREQ}}$ .
  - During SLEEP mode.
  - During  $\overline{\text{WAIT}}$  states.
- Refresh cycles are suppressed when the bus is released in response to  $\overline{\text{BUSREQ}}$ . However, the refresh timer continues to operate. The time at which the first refresh cycle occurs after the Z8S180/Z8L180 reacquires the bus depends on the refresh timer. This cycle has no timing relationship with the bus exchange.
- Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally latched (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and has no relationship with the exit from SLEEP mode.
- The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Thus, independent of the number of missed refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

MMU COMMON BASE REGISTER (CBR)

CBR specifies the base address (on 4 KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register

Mnemonic CBR

Address 38

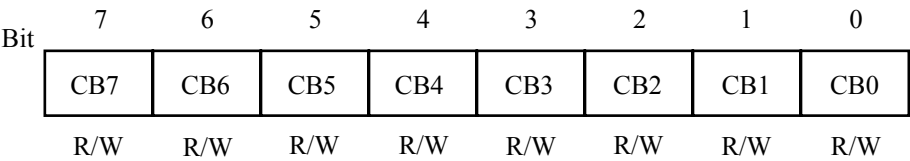


Figure 79. MMU Common Base Register (BBR: I/O Address = 38H)

MMU BANK BASE REGISTER (BBR)

BBR specifies the base address (on 4 KB boundaries) used to generate a 19-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register

Mnemonic BBR

Address 39

Bit	7	6	5	4	3	2	1	0
	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 80. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER (CBAR)

CBAR specifies boundaries within the Z8S180/Z8L180 64 KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

MMU Common/Bank Area Register

Mnemonic CBAR

Address 3A

MMU Common/Bank Area Register (CBAR: I/O Address = 3 AH)								
Bit	7	6	5	4	3	2	1	0
	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 81. MMU Common/Bank Area Register (CBAR: I/O Address = 3 AH)

**CA3–CA0 (Bits 7-4).** CA specifies the start (Low) address (on 4 KB boundaries) for the Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

**BA–BA0 (Bits 3-0).** BA specifies the start (Low) address (on 4 KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

Operation Mode Control Register

Mnemonic OMCR

Address 3E

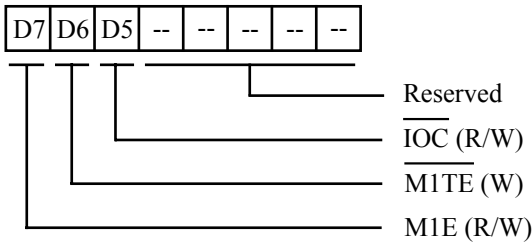


Figure 82. Operating Control Register (OMCR: I/O Address = 3EH)

**M1E (M1 Enable).** This bit controls the M1 output and is set to a 1 during reset.

When M1E=1, the  $\overline{\text{M1}}$  output is asserted Low during the opcode fetch cycle, the  $\overline{\text{INT0}}$  acknowledge cycle, and the first machine cycle of the NMI acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch an RETI instruction one time. When fetching an RETI from zero-wait-state memory, the processor uses three clock machine cycles which are not fully Z80-timing compatible but are compatible with the on-chip CTCs.

When M1E=0, the processor does not drive  $\overline{\text{M1}}$  Low during instruction fetch cycles. After fetching an RETI instruction one time with normal timing, the processor goes back and refetches the instruction using fully Z80-compatible cycles that include driving M1 Low. This may be required by some external Z80 peripherals to properly decode the RETI instruction.

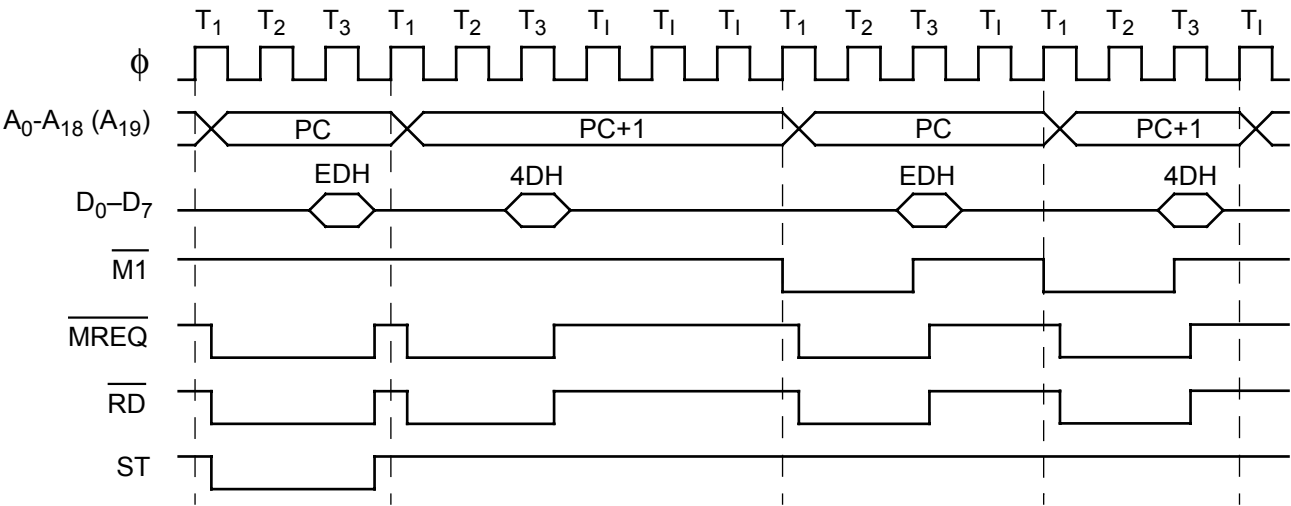


Figure 83. RETI Instruction Sequence with MIE=0

### I/O CONTROL REGISTER (ICR)

ICR allows relocating of the internal I/O addresses. ICR also controls enabling/disabling of the IOSTOP mode (Figure 84).

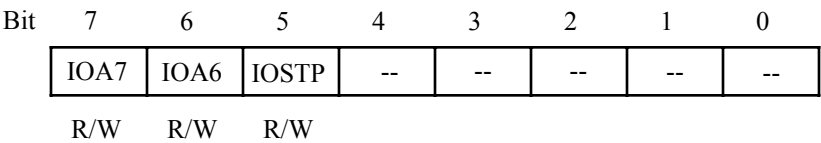


Figure 84. I/O Control Register (ICR: I/O Address = 3FH)

**IOA7, 6: I/O Address Relocation (bits 7,6).** IOA7 and IOA6 relocate internal I/O as indicated in Figure 85. Note that the high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.

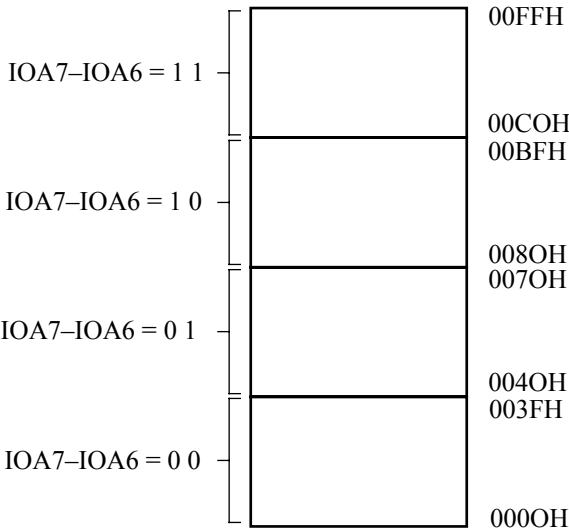


Figure 85. I/O Address Relocation

**IOSTP.** IOSTOP Mode (bit 5). IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTOP is reprogrammed or Reset to 0.

PACKAGE INFORMATION

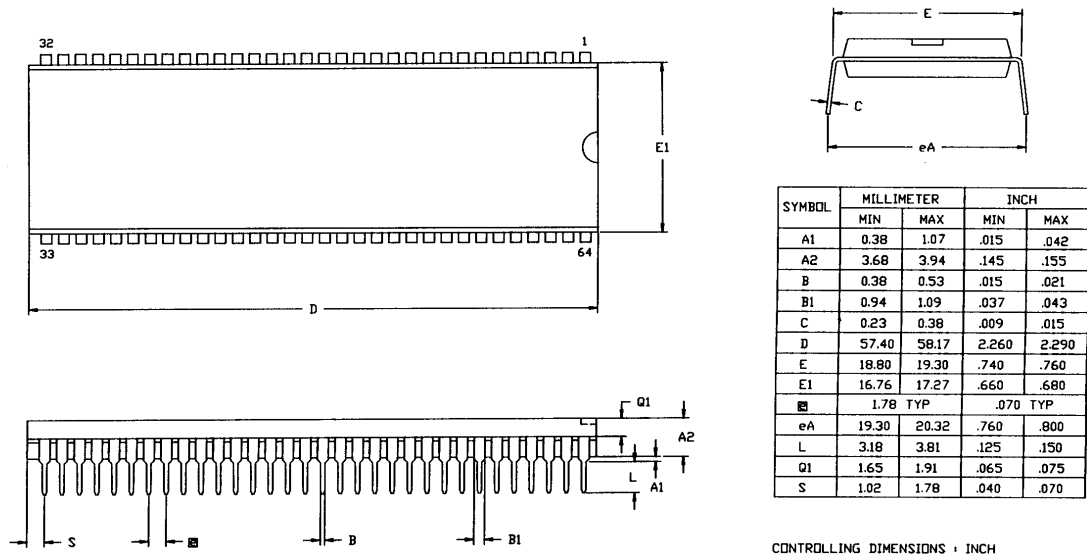


Figure 86. 64-Pin DIP Package Diagram

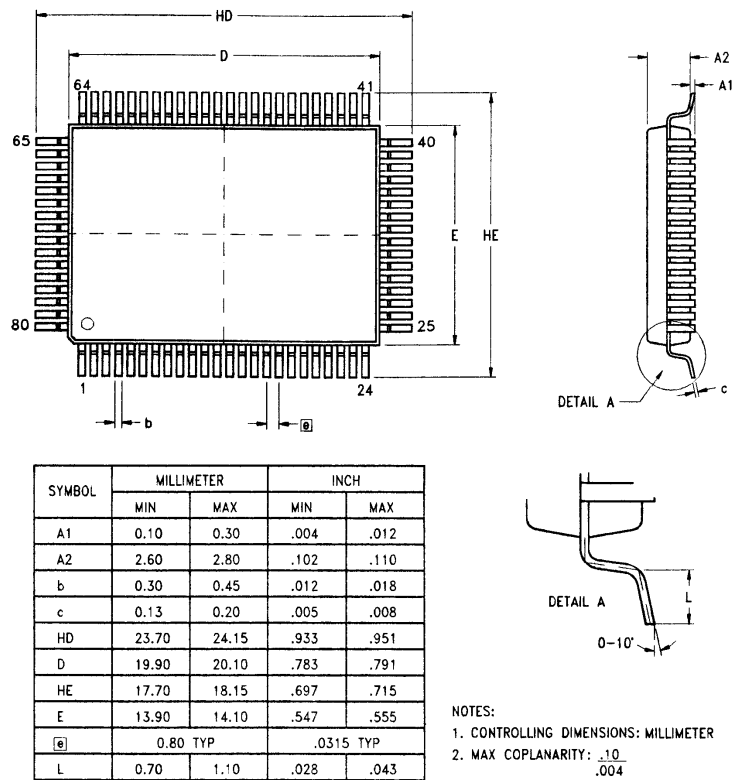


Figure 87. 80-Pin QFP Package Diagram

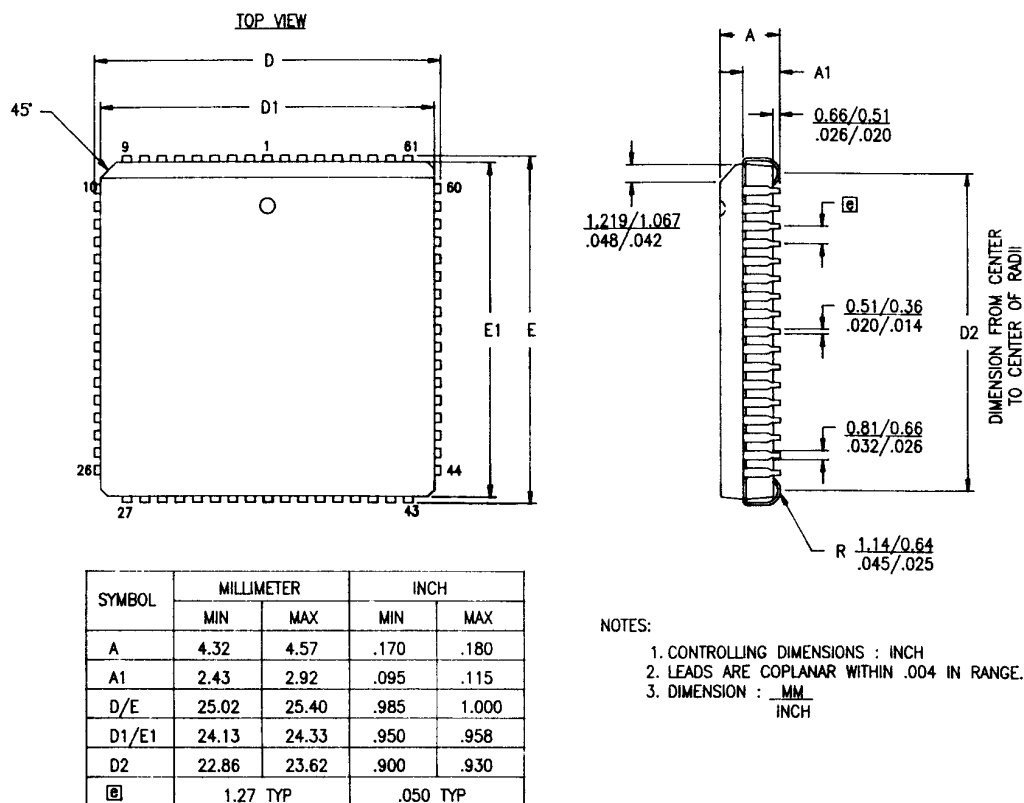


Figure 88. 68-Pin PLCC Package Diagram