Mem8Plus v2f Construction Notes

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Overview

All options for construction are listed here in the summaries. One way of building this board:

- Check off the options that are to be built here in the summaries.
- Then go down through the building instructions and cross off the components that do not correspond to the selected options. This will help guide the installation of the correct components for each option.
- As each component is installed, the checkbox can be checked to keep track of progress.

Mem8 options summary:

☐ M0 - Base RAM and ROM with supporting circuitry; 16-bit addressing; 5 volt operation (no regulators)
This is the base option for all builds and must be selected.
☐ M1 - 8 volt power using EZSBC regulator
☐ M2 - 8 volt power using Pololu regulator
☐ M3 - 24-bit addressing from S-100 bus
☐ M4 - ROM Wait-state generator
☐ M5 - Battery-backed RAM (currently not available)
☐ M6 - Memory Management Unit

Plus options summary:

☐ P0 - Monitor Base with LED displays for A0 to A15, DI0 to 7, DO0 to 7 and 15 significant status/control lines
☐ P1 - Main and Display boards are separated and connect with two 40-conductor cables
☐ P2 - 8 volt power using EZSBC regulator
☐ P3 - 8 volt power using Pololu regulator
☐ P4 - Base Hex displays - swaps hex displays for LED displays for all but status/control
☐ P5 - Extend LED address display to include A16 to A23
☐ P6 - Extended address hex displays - swaps hex displays for A16 to A23 LEDs
☐ P7 - Bank Select displays - adds LEDs to display bank selected by MMU
☐ P8 - Bank Select display LEDs swapped for hex display
☐ P9 - Front Panel - adds Run/Stop/Step, breakpoint, memory functions, program start features, etc. Uses dip switches for input.
☐ P10 - Change binary dip switches to rotary hexadecimal switches
☐ P11 - Add headers to accommodate user-provided off-board switches for data input and breakpoint address
☐ P12 - Extend address breakpoint to 24 bits using dip switch
☐ P13 - Change dip-switch in 24-bit extension to rotary hexadecimal switch
☐ P14 - Add header to accommodate off-board 24-bit address switches
☐ P15 - Control Pod - add header to accommodate user-supplied off-board switches on a panel or in a control pod, which can be used in place of the front-panel switches at the top of the Main Board.

Power Requirements depend on options selected. As designed, the Main board and the logic on the Display board all run off the main board power. The LEDs on the Display board run off the Display board power, using a separate regulator. For the hex display options, the hex displays and the LEDs run off the Display board regulator. With all options installed except the battery-backed RAM (which would be very low) and the 24-bit addressing option (two LS chips), the current drawn by the prototype was measured as such:

With the LED display board, Main board VCC current was 1.5A and Display Board LED+ current was 0.24A. LED+ current would probably be about 0.45A with all LEDs lit. With the hex Display board, Main board VCC current was 1.3A and LED+ current was 0.91A. Since the hex displays were all lit and operating, little increase would be expected in the LED+ current if all displays were indicating "8" (maximum LEDs lit in the displays.)

Board Build Procedure

There are numerous ways of assembling this board, and depending on the desired outcome and options selected, one way may be preferred over another. As the board is built and tested in steps, sometimes due to the interaction of the various options, a component must be installed temporarily. All these temporary components utilize existing empty IC sockets to accommodate. Care should be exercised when inserting temporary components not to stress the IC socket pins. Once the tests are completed, and assembly has continued, the temporary component (s) will be removed.

1. Using the BOM spreadsheet, determine which components will be needed for the options to be built. Collect all parts, ready for installation.
2. If it is known that the display board will not be needed, or it will be operated separated from the main board (option P1), it would be best to separate the two before any components are added.
3. Generally install components from "shortest" to "tallest". This lessens the chance of having to try to solder component leads on the back side of the board when disparately different height components are causing the board to be "wobbly."
4. A simple logic probe was built into the design, which can be used to help test and troubleshoot the board if no other test equipment is available. This feature is in option P0. However, if needed, it can be the first part of the board to be made operational in the testing procedure below.
5. Install discreet resistors (Incidentally, the convention here is to use the 'K' symbol as the decimal point. Hence, a 4700 ohm resistor will be denoted 4K7.):

    a. 4K7 1/4W:
    - ☐ M0: R1, R3, R5, R7
    - ☐ P9: R14

    b. 1K 1/4W:
    - ☐ M0: R2, R4, R6, R8

    c. 2K2 1/4W
    - ☐ P0: R75, R76

d. 270 1/4W
   ☐ P7 & not P8: R70, R71, R72, R73

e. 100K 1/4W:
   ☐ P9: R11, R15

f. 3K3 1/4W
   ☐ P9: R13

g. 47K 1/4W
   ☐ P9: R16

h. 10K 1/4W
   ☐ M0: R17, R18, R19, R22, R23, R24
   ☐ M0 & not M3: R21
   ☐ M0 & not M4: R20
   ☐ P9: R9, R10, R74

6. Install trimpot:
   a. 50K:
      ☐ P9: R12

7. Install monolithic ceramic capacitors:
   a. 0.1µF 25V:
      ☐ M0: C1, C2, C3, C5, C6, C7, C29, C42, C43, C45, C48, C54, C55, C56, C57, C59
      ☐ M3: C25, C53
      ☐ M4: C46
      ☐ M6: C26, C27, C28, C39
      ☐ P0: C33, C41, C70, C74, C76, C77, C80, C81, C88, C89, C90, C91, C92, C93
      ☐ P5: C71
      ☐ P9: C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C20, C24, C30, C31, C32, C34, C35, C37, C38, C40, C44, C50, C51, C52, C58, C78, C79, C82, C83, C84
      ☐ P12: C73, C75

   b. 0.01µF 25V:
      ☐ P9: C19

   c. 0.047µF 25V
      ☐ P9: C21

8. Install IC sockets:
   a. 8-pin:
      ☐ M5: U7, U8 (do not install - option currently not available)

- ☐ P9: U14

b. 14-pin:
   - ☐ M0: U5, U6, U40
   - ☐ M3: U18
   - ☐ P4: U79, U80, U83, U84, U90, U91, U93, U94
   - ☐ P6: U74, U75
   - ☐ P8: U70
   - ☐ P9: U12, U13, U15, U16, U17, U28, U29, U41

c. 16-pin:
   - ☐ M4: U42
   - ☐ M6: U21, U22
   - ☐ P0 & not P8: U71

d. 20-pin:
   - ☐ M0: U1, U3, U37, U38, U49, U50, U51, U52, U54
   - ☐ M3: U48
   - ☐ M6: U20, U30
   - ☐ P0: U24, U32, U95, U96
   - ☐ P0 & not P4: U77, U82, U89, U92
   - ☐ P5 & not P6: U72
   - ☐ P9: U23, U25, U27, U31, U33, U39, U45, U46, U47, U53, U78, U81, U85, U86
   - ☐ P12: U73, U76

e. 24-pin 0.3w:
   - ☐ M0: U2, U4
   - ☐ M6: U19
   - ☐ P9: U9, U10, U11, U26

f. 28-pin:
   - ☐ M0: U34

g. 32-pin:
   - ☐ M0: U35, U36

9. Install resistor networks:
   a. 4K7 10pin bussed:
      - ☐ M0: RN1, RN3
      - ☐ M3: RN4
      - ☐ M4: RN6
      - ☐ M6: RN5
      - ☐ P9: RN7

☐ P9 & not P10: RN75, RN77, RN79
with RN pin 1 to board pin 1, and set J74 & J75 to Active Low when installed later
☐ P9 & P10 (complementary hex switches): RN75, RN77, RN79
with RN pin 1 to board pin 1, and set J74 & J75 to Active Low when installed later
☐ P12 & not P13: RN76
with RN pin 1 to board pin 1

b. 1K 10 pin bussed:
☐ P9 & P10 (true hex switches): RN75, RN77, RN79
with RN pin 1 to board pin 11, and set J74 & J75 to Active High when installed later
☐ P12 & not P13: RN76
with RN pin 1 to board pin 11

c. 270 10 pin bussed:
☐ P0 & not P4: RN71, RN72, RN73, RN74, RN78, RN80
☐ P5 and not P6: RN70

d. 10K 10 pin bussed
☐ P9: RN2

e. 100K 10 pin isolated
☐ P9: RI1, RI2

10. Install switches:
a. 4-position dip:
☐ P9: S13

b. 8-position dip:
☐ M0: S1, S14
☐ P9 & not P10: S73, S82, S87
☐ P12 & not P13: S77

c. Rotary hexadecimal:
☐ P10: S71, S72, S80, S81, S85, S86
☐ P13: S75, S76

d. 4-position SPDT dip:
(Note: if the breakpoint “Don’t care” feature is not desired, these switches can be eliminated. Then they must be replaced by jumpers from switch pin 1 to 16, 3 to 14, and so on to force all bits normal.)
☐ P9: S79, S83, S84, S88
☐ P12: S74, S78

e. Momentary tactile:
☐ P9: S2, S3, S4, S5, S8

f. Miniature slide:
   - ☐ P0: S70
   - ☐ P9: S6, S7, S9, S10, S11, S12

11. Install electrolytic capacitors (observe polarity!):
    a. 0.47µF 25V
       - ☐ P9: C22

    b. 4.7µF 25V
       - ☐ P9: C23

    c. 10µF 25V
       - ☐ M0: C4, C36, C49, C60
       - ☐ P0: C73, C85, C87

    d. 47µF 25V
       - ☐ M0: C47
       - ☐ P0: C86

12. Install battery clips
    a. For type 2032 coin cell
       - ☐ M5: BT1, BT2 (Option currently not available - do not install)

13. Install discreet transistors
    a. 2N3906 plastic bipolar PNP
       - ☐ M0: Q1, Q2, Q3, Q4

14. Install headers
    a. 16-pin duel-row
       - ☐ M4: J10
       - ☐ M6: J9
       - ☐ P9: J12

    b. 8-pin duel-row
       - ☐ M3: J8

    c. 40-pin duel-row
       - ☐ P1: J1, J7, J79, J80

    d. 10-pin single-row
       - ☐ P11: J71, J77, J78
       - ☐ P14: J70

e. 12-pin single-row
   ☐ P15: J6

f. 3-pin single-row
   ☐ P9: J73 - J75

g. 5-pin single-row
   ☐ M2: U44
   ☐ P3: U88

h. 2-pin single-row
   ☐ M0: J13, J14, J15
   (Note: these jumpers add additional ground connections to the bus if the bus is configured thusly.)
   ☐ M0 & not M1: J11
   ☐ M0 & not M2: J11
   ☐ M0 & not M5: J2, J3, J4, J5
   ☐ M0 & not M6: J17, J18
   ☐ M0 & not P9: J19, J20, J21, J22, J23
   ☐ P0: J76
   ☐ P0 & not P2: J72
   ☐ P0 & not P3: J72

15. Install LEDs
    a. T1-3/4, color choice is up to builder
       ☐ P0: D68, D69, D70, D71, D71, D73, D74, D75, D76, D77, D78, D79, D80, D81, D82, D83
       ☐ P0 & not P4: D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D84, D85, D86, D87, D88, D89, D90, D91, D92, D93, D94, D95, D96, D97, D98, D99
       ☐ P5: D44, D45, D46, D47, D48, D49, D50, D51
       ☐ P7: D40, D41, D42, D43

16. Install power regulators
    a. EZSBC-PSU5 5 volt switching regulator
       ☐ M1: U43
       ☐ P2: U87

    b. Pololu D24V25F5 5 volt switching regulator
       ☐ M2: U44
       ☐ P3: U88

<u>Testing Procedure - Preliminary</u>

1. ☐ Carefully inspect the board for any poor connections, solder bridges or incorrect components.

2. ☐ Using an ohmmeter, measure resistance of +8 volt (or +5 volt) power input to 0 volt common. It should measure greater than 1KΩ.

3. ☐ If boards are separated, connect them with two 40-conductor cables. Length should not exceed 1 meter (3 ft).

4. ☐ Insert board into bus.

5. ☐ Connect a voltmeter across VCC and GND.

6. ☐ Power ON and measure 5 volts on both the main board and the display board. Any socket on the main board will be satisfactory, typically using the corner pins. For example, on a 20 pin chip, use pin 10 (GND) and pin 20 (VCC). On the display board, measure on any socket except the hex display sockets.

7. ☐ Measure 5 volts on the display board on any of the hex display sockets, pin 7 (GND) and pin 14 (LED+V).

8. ☐ Proceed only if the voltage measurements are good. If not, check the regulators and the power on the bus.

9. Optional Logic Probe checkout:
    a. ☐ Install IC U96 - 74LS240 (LED driver)
    b. ☐ Fabricate a simple, one-wire probe with a two-position header receptacle on one end and long enough to reach all points on the board. The wire goes to pin 1 of the connector and will plug into J76. The board is labeled TTL logic probe and is strictly for TTL level (0 to 5 volt) signals. The other end of the probe can be anything - a small alligator clip, a mini hook clip, even just tinned wire.
    c. ☐ Test the probe by touching the tip to any source of +5volts on the board. The Probe LED should light. Touch it to any ground point and the Probe LED should not light. Proceed after this simple test passes. Note that this will not detect a weak logic 1, e.g. a high-value pull-up. Also, if the signal being tested is pulsing, the LED will dim as a function of how much time the signal spends in the logic 1 state. A signal with infrequent low-going pulses may appear to be a logic 1; a signal with infrequent high-going pulses may appear to be a logic 0.

<u>Mem8 base RAM & ROM, option M0 (mandatory)</u>

1. Bringing this up will be easiest in a currently running system where various existing parts can be disabled. It will be done in two steps, first the RAM and then the ROM. If a currently running system is not available, then the testing of the RAM and ROM portions will best be accomplished at the same time.

2. Install the ICs and additional parts necessary to operate the RAM circuit for testing:
    a. ☐ U52 - 74LS244 (Data Out buffer)
    b. ☐ U37 - 74LS244 (Data Out to memory gate)
    c. ☐ U50 - 74LS244 (A0 - A7 buffer)
    d. ☐ U51 - 74LS244 (A8 - A15 buffer)
    e. ☐ U49 - 74LS244 (buffer for first half of the status and control signals)
    f. ☐ U54 - 74LS244 (buffer for second half of the status and control signals)
    g. ☐ U1 - GAL16V8 (RAM control - RAM)

h. ☐ U3 - GAL16V8 (I/O and misc. control - IOP)
i. ☐ Insert jumper shunts on J2, J3, J4 and J5. Even if the battery -backed RAM option is selected, test the RAM first without the option; ensure U7 and U8 are not installed.
j. ☐ U5 - 74LS04
k. ☐ U6 - 74LS125
l. ☐ U4 - GAL22V10 (Bus Control Logic - BCL)
m. ☐ Put jumper shunts on J19, J20, J21, J22 and J23. These are necessary to test the memory without the front-panel logic.

3. Temporary resistor needed to test the RAM without the ROM logic:
    a. ☐ Insert a 10K resistor at U2, pin 15 to 24. This will be removed at a later step.

4. Set the RAM dip-switch, S14, as follows :
    a. ☐ For 32K chip size, 1 & 2 are both open (or both 1, or both off, depending on switch nomenclature)
    b. ☐ For 128K chip size, 1 & 2 are closed and open respectively
    c. ☐ For 512K chip size, 1 & 2 are open and closed respectively
    d. ☐ Position 3 is closed
    e. ☐ Position 4 is closed
    f. ☐ Position 5 to 8 are irrelevant for now.

5. ☐ In this state, the board is only an S-100 bus listener and will not drive any signals on the bus. Without changing anything in the running system, insert the Mem8Plus, power up and start a program running, preferably one that attempts to read as much memory as possible. (Note: my Z80 Monitor running exercises all Address, Data Out and Control / Status signals except SOUT, which can be pulsed by hitting a key on the keyboard.)

6. ☐ With an oscilloscope or logic probe, verify that all <u>buffered</u> on-board bus signals appear to be moving:
    a. A0 - A15 (U50 pins 18, 16, 14, 12, 9, 7, 5 & 3; U51 pins 18, 16, 14, 12, 9, 7, 5 & 3)
    b. DO0 - DO7 (U52, pins 18, 16, 14, 12, 9, 7, 5 & 3)
    c. PSYNC, CLK, PDBIN, PWR*, SMEMR, SWO*, SINP, SOUT, SM1 (U49 pins 18, 16, 13 & 9; U54 pins 16, 14, 12, 9 & 7)

7. ☐ Confirm U3 pin 18 (SWO) and pin 19 (PWR) are moving.

8. ☐ Examine U1 pin 18 (ERAM1*) and pin 17 (ERAM2*). As your program is running, it should cause these two pins to pulse when reading the Mem8Plus address space.

9. ☐ Observe U36 pin 22 (M1CE*) and U35 pin 22 (M2CE*) for a moving signal.

10. ☐ Look at U35 or U36 pin 24 (RAMRD*) for a moving signal.

11. ☐ With a voltmeter, check for +5V at U35 and U36 pin 32. If chip size is 32K or 128K, check for +5V on pin30. If chip size is 512K, pin 30 is A17 and may be moving instead of a solid logic level.

12. ☐ Power down. Select one or two RAM chips to insert into the board at U36 and U35. If only one chip is being used, put it in U36. The board will accommodate 32K, 128K and 512K chips. This should be a similar amount of RAM as is currently in the computer.

13. ☐ Insert U38 - 74LS244 (Memory to Data In Gate)

14. ☐ Disable or remove the original memory from the computer.

15. ☐ Re-insert the Mem8Plus board and power-up.

16. ☐ If all is as expected, the computer should now be running on the Mem8Plus RAM.

17. ☐ If not, various troubleshooting steps can be employed to find and correct the problem:
    a. Is the RAM good? Can it be verified in another board or computer?
    b. Were the GALs programmed properly? Previous tests should have uncovered issues, but confirmation would be good.
    c. Are the dip-switches and jumpers set properly?
    d. Are the jumpers and temporary resistor described above installed?
    e. Carefully re-inspect the board for poor solder joints or solder bridges.
    f. Retest. Continue troubleshooting until it works.

18. ☐ Next the ROM circuit will be checked out. It is assumed that a ROM or EPROM is available and programmed with some sort of basic monitor program; perhaps a copy of the chip in the original computer memory board. Note the size of the chip. It is most likely a 2716 or similar 2K chip, a 2732 or similar 4K chip, a 2764 or similar 8K chip or a 27128 or similar 16K chip. The Mem8Plus supports all four of these sizes.

19. ☐ Insert U40 - 74LS136 (Open-collector bus driver)

20. ☐ Set the ROM dip switch S1, positions 4 and 5, as follows:
    a. 2K ROM - closed (or 0 or ON), closed
    b. 4K ROM - open, closed
    c. 8K ROM - closed, open
    d. 16K ROM - open, open

21. ☐ Set the ROM dip switch S1, positions 1, 2 and 3 to indicate the start of the ROM:
    a. 8000H - closed, closed, closed
    b. 9000H - closed, closed, open
    c. A000H - closed, open, closed
    d. B000H - closed, open, open
    e. C000H - open, closed, closed
    f. D000H - open, closed, open
    g. E000H - open, open, closed
    h. F000H - open, open, open

22. ☐ Set the ROM dip switch S1, position 6 to open and position 7 to closed (position 8 is irrelevant). This is ROM option 2 - ROM always ON in bank 0 (assuming no 24-bit external address option.)

23. ☐ Remove the temporary resistor at U2, and insert U2 - GAL22V10 (ROM control logic - ROM)

24. ☐ Insert the EPROM in U34.

25. ☐ Disable the ROM that was running in the computer prior to the Mem8Plus.

26. ☐ Insert the Mem8Plus board back into the computer and power-up.

27. ☐ The ROM on the Mem8Plus should run the firmware now.

28. ☐ If not, various troubleshooting steps can be employed to find and correct the problem:
    a. Dip-switches are set properly.
    b. ROM GAL (U2) was programmed properly.
    c. ROM was properly inserted in to the socket.
    d. It is possible that the ROM is too slow and may need the wait-state generator option.
    e. Continue troubleshooting until it works.

<u>Mem8 Power Regulator, EZSBC, option M1</u>

When using this option, be sure to remove J11.
Confirmation of this option was done in the preliminary tests.

<u>Mem8 Power Regulator, Pololu, option M2</u>

When using this option, be sure to remove J11.
Confirmation of this option was done in the preliminary tests.

<u>Mem8 24-bit Addressing, option M3</u>

1. ☐ Insert U48 - 74LS244 (Address A16 - A23 buffer)

2. ☐ Insert U18 - 74LS136 (Address Decoder)

3. ☐ With shorting shunts, select the binary board address on J8. A jumper on selects that bit high. The board can be addressed at any one of 16 addresses from 0xxxxH to FxxxxH.

4. ☐ Insert board in bus and power-On.

5. ☐ Using a CPU capable of addressing more than 64K, and appropriate software, verify that memory can be read and written. (Note: this option was not tested on the prototype as a CPU with this capability was not available.)

Mem8 ROM Wait State, option M4

1. ☐ Insert U42 - 74LS165 (8-bit shift register - counts wait states)

2. ☐ With shorting shunts, select the desired number of wait-states on J10. No shunts for zero wait states. Add one shunt at "1" to get one wait state. Add a second shunt at "2" for two wait states. Continue adding shunts for up to eight wait states. Note that all subsequent shunts remain in place as more are added for additional wait states.

3. ☐ Insert the board into the bus and power On.

4. ☐ With at least one wait state set, confirm activity on U42 pin 9 as evidence that ROM wait states are being produced. If an oscilloscope is available, view a waveform on U42 pin 9. Add shunts and watch the duty cycle change to indicate more wait states.

Mem8 Battery-backed (non-volatile) RAM, option M5

This option is currently not available. A design problem surfaced in prototype testing. If this option is used along with the automatic chip configuration circuit, the batteries are drained very quickly. A correction has been designed, but it is not easy to patch in. The next major revision should have the problem corrected.

Mem8 Memory Management Unit (MMU), option M6

Note: it will be easier to test this option if option P7 or option P8 (bank select display) are selected and installed first. Also helpful are options P5 or P6 (A16 - A23 display). Of course, these options require option P0, which must be selected and installed as well ahead of option M6.

1. ☐ Insert U30 - 74LS688 (MMU I/O port decoder)

2. ☐ Using jumper shunts at J9, select an appropriate I/O address for the MMU bank select port. A shunt ON programs a low for that bit. For example, to select output port 32H (0011 0010 binary), put shunts on A7, A6, A3, A2 and A0.

3. ☐ Put the board into the bus and power ON. Using a monitor program, output anything to the port selected above. Observe a pulse on U22 pin 9.

4. ☐ Insert U22 - 74LS174 (MMU Bank Select Register)

5. ☐ Put the board into the bus and power ON. Using a monitor program, output 01H to the MMU bank select port setup in step four above. Observe the outputs of U22, pins 10, 7, 5 and 2 with a logic probe. The pattern 0001

should be seen. Send various combinations of bits to the bank select port and be sure the output of U22 agrees. Note that if the Bank Select LED display, option P7 or the Bank Select Hex display, Option P8 was constructed prior, the bank select register output will show on these displays.

6. ☐ Remove jumper shunts from J17 and J18.

7. Insert components:
    a. ☐ U20 - 74LS244 (MMU A16 - A23 bus driver)
    b. ☐ U19 - GAL22V10 (MMU logic - MMU)

8. ☐ Set dip switch S14, positions 5, 6 and 7:
    a. Position 5 and 6 set the common size; choose one and set it.
    The correct common size is a function of the OS and its configuration.
    For testing, any common size should be satisfactory, but note the setting for use below.
    Closed, Closed (0, 0) is 8K
    Open, Closed (1, 0) is 16K
    Closed, Open (0, 1) is 24K
    Open, Open (1, 1) is 32K
    b. Position 7 sets the bank select mode - open (1) is normal, closed (0) is encoded.
    Normal mode corresponds to the Cromemco bank select scheme where each bit can select one bank.
    For example, if 0001H is set in the bank select register, then bank 1 is selected.
    Bank 2 is 0010H, bank 3 is 0100H, and bank 4 is 1000H.
    Only one high bit is permitted at any one time; only four banks can be selected.
    Encoded mode permits up to 16 banks to be selected, one at a time.
    In this mode, any bit can be high at any time, so 0001H is bank 1, and bank 2 is 0010H as before.
    But bank three is 0011H and bank 4 is 0100H. 1000H is bank 8 and 1111H is bank 16.
    For testing, the mode will be set to normal.

9. Note that with 16 possible banks, the maximum RAM addressable is 1MB, which also happens to be the maximum RAM the board can contain (2 x 512K chips). As such, address lines A20 to A23 will always be driven low out of the MMU logic and there is concern for only A16 to A19. The MMU logic can be summarized and explained best with a truth table. This shows only the logic associated with normal mode:

Criteria					CommonSiz		Address Bits			Select Bits				Outputs						
Bank	ComSiz	CPUAddr	Operation	BSRS	CS1	CS0	A15	A14	A13	B3	B2	B1	B0	RBNK	LOBNK	HIBNK	A19	A18	A17	A16
0	any	any	After reset, before BS reg wrt	0	x	x	x	x	x	x	x	x	x	1	0	0	0	0	0	0
1	any	00 - FF	Bank 1 - "normal" 1 of 4 BS bits	1	x	x	x	x	x	0	0	0	1	0	1	0	0	0	0	0
2	any	00 - 7F	Bank 2	1	x	x	0	x	x	0	0	1	0	0	0	0	0	0	0	1
2	32K	80 - FF	Common	1	1	1	1	x	x	0	0	1	0	0	1	0	0	0	0	0
2	24K	A0 - FF	Common	1	1	0	1	0	1	0	0	1	0	0	1	0	0	0	0	0
2	24K	80 - 9F	Bank 2	1	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1
2	16K	C0 - FF	Common	1	0	1	1	1	x	0	0	1	0	0	1	0	0	0	0	0
2	16K	80 - BF	Bank 2	1	0	1	1	0	x	0	0	1	0	0	0	0	0	0	0	1
2	8K	E0 - FF	Common	1	0	0	1	1	1	0	0	1	0	0	1	0	0	0	0	0
2	8K	80 - DF	Bank 2	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	1
3	any	00 - 7F	Bank 3	1	x	x	0	x	x	0	1	0	0	0	0	0	0	0	1	0
3	32K	80 - FF	Common	1	1	1	1	x	x	0	1	0	0	0	1	0	0	0	0	0
3	24K	A0 - FF	Common	1	1	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0
3	24K	80 - 9F	Bank 3	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0
3	16K	C0 - FF	Common	1	0	1	1	1	x	0	1	0	0	0	1	0	0	0	0	0
3	16K	80 - BF	Bank 3	1	0	1	1	0	x	0	1	0	0	0	0	0	0	0	1	0
3	8K	E0 - FF	Common	1	0	0	1	1	1	0	1	0	0	0	1	0	0	0	0	0
3	8K	80 - DF	Bank 3	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	1	0
4	any	00 - 7F	Bank 4	1	x	x	0	x	x	1	0	0	0	0	0	1	0	0	1	1
4	32K	80 - FF	Common	1	1	1	1	x	x	1	0	0	0	0	1	0	0	0	0	0
4	24K	A0 - FF	Common	1	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0
4	24K	80 - 9F	Bank 4	1	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1	1
4	16K	C0 - FF	Common	1	0	1	1	1	x	1	0	0	0	0	1	0	0	0	0	0
4	16K	80 - BF	Bank 4	1	0	1	1	0	x	1	0	0	0	0	0	1	0	0	1	1
4	8K	E0 - FF	Common	1	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0
4	8K	80 - DF	Bank 4	1	0	0	1	1	0	1	0	0	0	0	0	1	0	0	1	1

At reset or power-on, the BSRS bit from the bank register forces the MMU logic to the reset state, called bank 0. All inputs are ignored, A16 - A19 are driven low and the RBNK signal to the ROM logic enables the ROM. In the course of normal operations, perhaps by the boot loader, a write to the Bank select register, typically a 01H for selecting bank 1, sets BSRS, enabling the MMU logic and subsequently setting RBNK low disabling the ROM. Bank 1 is the “normal” bank of 64K with A16 to A19 low. By writing a different bit high in the bank select register, and depending on the setting of the common size dip switch, the logic will select a different memory region above 64K to substitute for low memory. For example, if the common size is 16K, then physical address C000 to FFFF will always address “common” bank 1 memory (A16 - A19 are 0000), and physical address 0000 to BFFF will come from bank 2 memory (A19 - A16 are 0001). Bank-switching back to bank 1 will return physical address 0000 to BFFF back to bank 1.

Operation of the MMU logic for the Encoded mode is identical, except the Select Bits B0 to B3 from the bank select register are decoded into 1 of 16 possible banks and the truth table is four times as long. Also, like in normal mode, HiBnk will be true only when the top bank of RAM is selected.

10. ☐ Put the board into the bus and power ON.

11. ☐ With a monitor program, output 01H to the bank select port selected in step 3 above. If one of the bank select display options is operating, observe this on the display, else use a logic probe to confirm. It may be possible that A16 to A23 will no longer be 00H, (see on display or logic probe) and it is also possible that the computer will crash. This is because the bank select operation has disrupted the monitor’s memory space - a good sign that the MMU is working. If the monitor is still running, attempt to read memory from a non-common address. Regardless of the common setting, reading from 2000H is outside the common memory space. Now the A16 to A23 display should

show something other than 00H, a sign that the MMU is working. With so many possibilities, it will not be possible to test them all. If one works, then all should be fine.

Mem8Plus Bus Monitor Base, option P0 without option P4

This is the base bus monitor option utilizing binary LED displays grouped into bytes. Option P4 is the same board populated instead with hexadecimal displays. The two options are mutually exclusive. If the P4 option is to be built, skip these steps and go directly to the P4 option section below.

1. Insert these components for the Monitor Display:
    a. ☐ U32 - 74LS244 (Data In Bus to display)
    b. ☐ U89 - 74LS240 (DI0 - DI7 LED driver)
    c. ☐ U24 - 74LS244 (Data Out Bus to display)
    d. ☐ U92 - 74LS240 (DO0 - DO7 LED driver)
    e. ☐ U77 - 74LS240 (A8 - A15 LED driver)
    f. ☐ U82 - 74LS240 (A0 - A7 LED driver)
    g. ☐ U95 - 74LS240 (Status LED driver)
    h. ☐ U96 - 74LS240 (Control LED driver - may already be installed from logic probe assembly)

2. ☐ Set S70 to ON.

3. ☐ Put the board into the bus, power ON and confirm that the Display are functional.

4. ☐ Slide the Displays switch, S70, to the OFF position and confirm that the displays go OFF. Then return the switch to the ON position.

Mem8Plus Separate Display Board, option P1

This option is best exercised before any components are installed. However, if care is taken, the boards can still be separated afterwards.

1. ☐ To separate the boards, note that perforations were made during board fabrication between the two boards. Using a sharp knife (like a utility knife or an “X-acto” knife), run the length of the perforations with the blade, especially in the areas where the runs connect the two boards. Do this several times to score the perforations and ensure that the runs are cut. Then using diagonal cutters start the break on both ends of the perforation. With it started, the boards ought to snap apart.

2. ☐ Install four 40-pin 0.1” duel-row headers at J1, J7, J79 and J80. These can be installed on either side of either board to accommodate physical needs. Just be sure to match up pin 1 to pin 1.

3. ☐ Obtain or fabricate two 40-conductor cables with 40-pin header receptacles on each end. (Similar to PATA cables for IDE disk drives.) These can be as long as desired, but at some point they will not work (this point has not been

determined - 18” is about as long as has been tested.)

4. ☐ Connect both 40-pin cables, power-ON and test.

Mem8Plus Power Regulator, EZSBC, option P2

When using this option, be sure to remove J72.
Confirmation of this option was done in the preliminary tests.

Mem8Plus Power Regulator, Pololu, option P3

When using this option, be sure to remove J72.
Confirmation of this option was done in the preliminary tests.

Mem8Plus Base Hex Display, option P4

1. Insert these components for the Data In and Data Out Display:
    a. ☐ U90, U91 - TIL311 (Data In Bus hex display)
    b. ☐ U93, U94 - TIL311 (Data Out Bus / Outport hex display)

2. Insert these components for the Address Display:
    a. ☐ U79, U80 - TIL311 (A8 - A15 hex display)
    b. ☐ U83, U84 - TIL311 (A0 - A7 hex display)

3. Insert these components for the Status and Control Display:
    a. ☐ U95 - 74LS240 (Status LED driver)
    b. ☐ U96 - 74LS240 (Control LED driver - may already be installed from logic probe assembly)

4. ☐ Set S70 to ON.

5. ☐ Put the board into the bus, power ON and confirm that the Data In, Data Out, Address and Status/Control Displays are functional.

6. ☐ Slide the Display switch, S70, to the OFF position and confirm that the displays go OFF. Then return the switch to the ON position.

Mem8Plus LED display for Address bus A16 - A23, option P5

1. ☐ Insert U72 - 74LS240 (A16 - A23 LED driver)

2. ☐ Put the board into the bus, power ON and confirm that the A16 to A23 LEDs are functional. This option requires the M3 or M6 option to produce anything meaningful on the display.

Mem8Plus Hex display for Address bus A16 - A23, option P6

1. ☐ Insert U74 and U75 - TIL311 (A16 - A23 hex display)

2. ☐ Put the board into the bus, power ON and confirm that the A16 to A23 displays are functional.

Mem8Plus LED display for Bank Select, option P7

1. ☐ Insert U71 - 74LS368 (Bank Select LED driver)

2. ☐ Put the board into the bus, power ON and confirm that the bank select LED display is functional. This option requires the M6 option to produce anything other than "0" (no LEDs lit) on the display. Then software is required to write something other than 0 to the bank select port.

Mem8Plus Hex display for Bank Select, option P8

3. ☐ Insert U70 - TIL311 (hex display)

4. ☐ Put the board into the bus, power ON and confirm that the bank select hex display is functional. This option requires the M6 option to produce anything other than "0" on the display. Then software is required to write something other than 0 to the bank select port.

Front Panel, option P9

1. ☐ Remove jumper J19.

2. ☐ Insert U12 & U13 - both 74HCT14 (switch buffer and de-bounce)

3. ☐ Set the slide switches as follows:
    a. S6 - Normal
    b. S7 - Run
    c. S9 - M1
    d. S10 - Off
    e. S11 - Off
    f. S12 - DispDO

4. ☐ Put the board into the bus and power ON.

5. ☐ With a logic probe, observe the outputs of the HCT14's while the corresponding switch is cycled. The output should move to the opposite state when the switch is changed, and return when the switch returns. Here is a chart to help check these outputs showing the Reference Designator and pin number, the full name and the board label:
    a. U13-2: Memory Examine - MemEx
    b. U13-4: Memory Examine Next - MemExNxt
    c. U13-6: Memory Deposit - Deposit
    d. U13-8: Memory Deposit Next - DepNxt
    e. U13-10: Control Mode: Normal/FrontPanel - Normal/FPnl
    f. U13-12: CPU Run/Stop - Run/Stop
    g. U12-2: Step One Cycle - Step
    h. U12-4: Step Type: AnyCycle/M1Only - Any/M1
    i. U12-6: SlowStep OFF/ON - Slwstp/Off
    j. U12-8: Breakpoint Off/Armed - BPOn/Off
    k. U12-12: OutputDisplay: Outpot/DO Bus - DispTP/DispDO

6. ☐ Insert U14 - 555 (Slow-step oscillator)

7. ☐ Put the board into the bus and power ON.

8. ☐ Set Dip Switch S13, all positions ON

9. ☐ Set R12 to about mid-range.

10. ☐ With a logic probe, observe U14 pin 3 for a pulsing output.

11. ☐ Take a minute to see the effects of adjusting R12 and switching in and out the various resistors and capacitors with dip switch S13.

12. ☐ Insert a temporary 10K resistor @ U86 pin 20 to 19.

13. Insert the following components of the Run/Stop Step circuit:
    a. ☐ U17 - 74LS74 (HoldStop and Stp1cycle flip-flops)
    b. ☐ U28 - 74LS74 (RunCont and sync flip-flops)
    c. ☐ U29 - 74LS74 (Breakpoint latch and sync flip-flop)
    d. ☐ U41 - 74LS20 (Run/Stop Master Latch)
    e. ☐ U27 - GAL16V8 (Run/Stop/Step logic - RSL)

14. ☐ Ensure the Front Panel slide switches are set as follows:
    a. S6 - Normal
    b. S7 - Run
    c. S9 - M1
    d. S10 - Off

e. S11 - Off
f. S12 - DispDO

15. ☐ Put the board into the bus and power ON.

16. ☐ The ROM Monitor should run as usual. Test the Run / Stop / Step functions:
    a. ☐ Move the Run/Stop switch to Stop. The CPU should stop and all displays become static.
    b. ☐ Press the Step button. The CPU should step to the next M1 instruction and display the address on the address display, the data on the data out display and control/status on those LEDs. If a listing of the monitor program is available, one can follow along and watch the program execute one instruction at a time.
    c. ☐ Move the Any/M1 switch to Any.
    d. ☐ Press the Step button. The CPU should advance to the next M state. This won't necessarily be an M1 state. Any M state will be visible, including Memory Read, Memory Write, Port Read, Port Write and Interrupt Acknowledge. Observe the Status and Control LEDs to see what M state the CPU is in.
    e. ☐ Move the SlwStp switch to the SlwStp position. The CPU will step (run) at a frequency determined by the slow-step oscillator that was checked-out above. Of course, changing the dip-switch and the variable resistor will change the speed of execution.
    f. ☐ Move the SlwStp switch back to off and slow-step execution will stop.
    g. ☐ Move the Run/Stop switch back to Run and the CPU will return to normal full-speed operation.
    h. ☐ Switch back to Stop. Reset the computer. Note that the CPU comes up in the stopped state.
    i. ☐ Switch back to Run. Reset the computer. Note that the CPU comes up in the running state.

17. Insert the following components of the Test I/O Port circuit:
    a. ☐ U31 - 74LS688 (Port address comparator/decoder)
    b. ☐ U45 - 74LS244 (Test Input port gate)
    c. ☐ U23 - 74LS374 (Test Output port latch)

18. Place jumper shunts on J12, "Test I/O Port Addr. Config" to select a port address for the Test I/O Port. A shunt ON programs a low for that bit. For example, to select output port 32H (0011 0010 binary), put shunts on A7, A6, A3, A2 and A0.

19. ☐ Put the board into the bus and power ON.

20. ☐ Set switch S12 to DispTP.

21. ☐ Using a monitor program or similar, output a byte to the port selected on J12 above. Observe the byte output on the Data Out Buss / Outport display. Try sending various bytes to see that all bits function.

22. ☐ Switch S12 back to DispDO to see the Data Out Bus again.

23. ☐ Using a monitor program or similar, input a byte from the port selected on J12 above. The byte set in the Data In dip switch, S73 will be read in. Try setting various numbers on the dip switch and ensure that it is always read correctly.

24. Insert the following components of the Hardware Breakpoint circuit:
    a. ☐ U81 - 74LS688 (Address Comparator for A8 - A15)
    b. ☐ U86 - 74LS688 (Address Comparator for A7 - A0)
    c. ☐ @J73 - Jumper shunt set for 16-bit Compare

25. ☐ Set all SPDT Breakpoint Compare switches (S74, S78, S79, S83, S84 & S88) to “Normal”.

26. ☐ Set Breakpoint Address switch S82 to hex 01, or binary 00000001.

27. ☐ Set Breakpoint Address switch S87 to hex 00, or binary 00000000.

28. ☐ Put the board into the bus and power ON.

29. ☐ Using a monitor program or similar with the capability of changing memory and running programs, enter this very simple Z80 (or 8080) program into memory at 0100H:
    JP 0100
    In machine language, this would be C3 00 01.
    When executed, it will just spin in a very tight loop, jumping back to itself.

30. ☐ Now execute the program. The computer will seem to freeze, however some activity may be observable on address, data or status/control displays.

31. ☐ Switch the BreakPoint Enable switch, S11 to BPOn. This should trigger the breakpoint and stop the CPU.

32. ☐ Set S9 to Any, move the Run/Stop Switch to Stop, and set the Breakpoint enable switch to OFF.

33. ☐ Press the Step switch a number of times and confirm that the computer is indeed executing three M states. Address 0100H is a M1 Read of the opcode C3 , address 0101H is a Memory Read of the low address operand 00, and 0102H is a Memory Read of the high address operand 01. Then it returns to 0100H to do it all over again.

34. The design of a test for the Breakpoint “Don’t Care” switches is in progress.

35. ☐ Remove jumper J21.

36. Insert the following components of the Front Panel mode Memory Examine and Deposit circuit:
    a. ☐ U15 - 74LS74 (Switch state latch)
    b. ☐ U16 - 74LS74 (Switch state latch)
    c. ☐ U26 - GAL22V10 (Front Panel Logic - FPL)
    d. ☐ U9, U10 & U11 - GAL22V10 (Memory Examine Address Registers - FPR; all three GALs are identical)
    e. ☐ U33 - 74LS244 (Data Switch to memory gate)
    f. ☐ U78 - 74LS244 (A8 - A15 Switch buffer)
    g. ☐ U85 - 74LS244 (A0 - A7 Switch buffer)

37. ☐ Ensure Front Panel Mode switch (S6) is set to Normal, and Run/Stop switch (S7) is set to Run.

38. ☐ Put the board into the bus and power ON. Observe normal operation. Note that even if the 24-bit or the MMU options are not present, the Front Panel option is always a 24-bit operation, dependent on memory population.

39. ☐ Switch Run/Stop to Stop. CPU stops. The contents of the data and address displays will be arbitrary.

40. ☐ Switch Front Panel Mode Switch to FPnl. The four Memory Examine and Deposit switches now become active for front-panel operations, and the Breakpoint set switches are utilized as address input switches. Perform this exercise to test their functions:
    a. ☐ Set the address input (BP) switches: A23 - A16 = 00H, A15 - A8 = 01H, A7 - A0 = 00H.
    b. ☐ Press MemEx. The address bus display should show 00 01 00 (00000000 00000001 00000000). The data display will show the contents of memory at this address.
    c. ☐ Press MemExNxt. The address bus should increment and show the next memory location contents.
    d. ☐ Repeatedly pressing MemExNxt will examine up through memory.
    e. ☐ Press MemEx to return to 00 01 00.
    f. ☐ Using the data input switch, S73, set any bit pattern.
    g. ☐ Press Deposit. The data display will show the bit pattern set on the data input switch.
    h. ☐ Press MemExNxt and observe a different bit pattern.
    i. ☐ Press MemEx to return to 00 01 00. The bit pattern set on the data switches returns to the display, showing that the deposit function wrote the bit pattern to memory.
    j. ☐ Press MemExNxt to get to 00 01 01.
    k. ☐ Set a different bit pattern on the data switches. Press DepNxt. The data input does not show on the data display, but rather the contents of the memory at the next address. Deposit Next is like pressing deposit following immediately by pressing Examine Next.
    l. ☐ Set another bit pattern on the data switches and press DepNxt.
    m. ☐ Press MemEx to return to 00 01 00.
    n. ☐ Press MemExNxt to step up through memory to observe the bit patterns put there by Deposit Next.
    o. Summary of Front Panel Memory operations:
    Examine Memory (MemEx) reads the Address switches and shows the memory contents of that address.
    Memory Examine Next (MemExNxt) increments to the next memory address and shows the contents.
    Deposit (Deposit) reads the contents of the Data In switches and puts that into the current memory addr.
    Deposit Next (DepNxt) does a deposit and immediately a Memory Examine Next.

41. ☐ Remove jumpers J22 and J23.

42. Insert the following components of the Program Start circuit:
    a. ☐ U21 - 74LS367 (Bank gate)
    b. ☐ U46 - 74LS374 (Address Lo Register)
    c. ☐ U47 - 74LS374 (Address Hi Register)
    d. ☐ U53 - 74LS244 (Jump Gate)
    e. ☐ U25 - GAL16V8 (Program Start Logic #1 - PSS)
    f. ☐ U39 - GAL16V8 (Program Start Logic #2 - PSL)

43. The Program Start circuit utilizes the data input switch, S73 (or S71 & S72 if the hex switch option is installed), and re-purposed MemEx, MemExNxt and Deposit switches to load a start address into the Program Start registers. Then the DepNxt Switch is re-purposed as a go button that forces the CPU to the address set in the Program Start registers. The next exercise will step through the process and ensure that the feature is working properly.

44. ☐ With the system operating normally in the ROM monitor or similar program, ensure the Normal/FPnl switch is set to Normal and the Run/Stop switch is set to Run.

45. ☐ Check to be sure the Step Type switch is set to M1.

46. ☐ Move the Run/Stop switch to Stop. The CPU will stop at an arbitrary address in the M1 instruction fetch cycle.

47. ☐ Enter the bank of the desired jump target into the Data Input switches, and then press MemEx. The bank display (if constructed) will show the bank entered on the switches.

48. ☐ Enter the A15 - A8 half of the desired jump target into the Data Input switches. (A good test might be to setup the start address of the monitor ROM. Then at the end of the test, the beginning of the ROM can be observed to validate operation.) Then press MemExNxt. Nothing shows on the display.

49. ☐ Enter the A7 - A0 half of the desired jump target into the Data Input switches. Then press Deposit. Nothing shows on the display.

50. ☐ Move the Step Type switch to Any.

51. ☐ Press the DepNxt button and observe hex C3 (binary 1100 0011) on the Data display.

52. ☐ Press Step. This causes the CPU to read the C3 as the opcode of the next instruction. Of course, C3 is a Jump. You may also notice the Address Display increment. This is irrelevant as the CPU is currently not addressing memory.

53. ☐ Press the DepNxt button and observe the low half of the jump target address entered above.

54. ☐ Press Step. This causes the CPU to read the low half of the jump target address. As before, the address may increment.

55. ☐ Press DepNxt button and observe the high half of the jump target address entered above.

56. ☐ Press Step. This causes the CPU to read the high half of the jump target address.

57. ☐ Press DepNxt button a fourth time to end the Program Load sequence and return control back to the CPU. The CPU should still be stopped in the M1 state. The jump target address should now be displayed in the address display and the contents of memory at the jump target address should be on the data display. If the start address of the monitor ROM was used as the jump target, check to see that the data displayed is indeed the first byte of the ROM.

58. ☐ At this point, the Front Panel logic is in a normal stopped CPU state. From here, the user may single step the code by pressing Step, Slow-step the code by setting S10 to SlwStep, set an optional breakpoint and then arm breakpoints and/or set the Run/Stop switch to Run to execute the code at the displayed address at full speed.

Hex Switches, option P10

This is only a board construction option. It substitutes rotary hexadecimal switches for binary dip switches. The rotary switches are much simpler to set than dip switches and read directly in hex. Otherwise they are functionally equivalent to dip switches. There is nothing specific to test that does not get tested in option P9 tests.

External Address and Data Switches, option P11

This is only a board construction option. It simply adds headers to the board so external switches can be added. The external switches can co-exist with the on-board switches, but the unused ones must be set to off, or the position that would be the same as if they were not installed.

24-bit Address Comparator, option P12

This option extends the capability of the breakpoint hardware to 24 bits.

1. Insert these components for this option:
    a. ☐ U73 - 74LS244 (Address bus buffer and gate)
    b. ☐ U76 - 74LS688 (Bus comparator)

2. ☐ Set J73, Address Compare Length, to 24-bit

3. ☐ Put the board into the bus and power ON.

4. ☐ Set a 24-bit address on the dip or hex switches that corresponds to an address in software that can be run. Arm the breakpoint with S11 (BPOn). Run the program that accesses the address set and observe the program break with the break address on the address display. (Note that this option was not tested on the prototype due to the lack of a CPU with 24-bit address capability.)

24-bit Hex Switches, option P13

This is only a board construction option. It substitutes rotary hexadecimal switches for binary dip switches. The rotary switches are much simpler to set than dip switches and read directly in hex. Otherwise they are functionally equivalent to dip switches. There is nothing specific to test that does not get tested in option P12 tests.

24-bit External Switches, option P14

This is only a board construction option. It simply adds a headers to the board so external switches can be added. The external switches can co-exist with the on-board switches, but the unused ones must be set to off, or the position that would be the same as if they were not installed.

External Front-Panel (Control Pod) switches, option P15

This is only a board construction option. It simply adds a header to the main board so external front panel control switches can be added. The external switches can co-exist with the on-board switches, but the unused ones must be set to off, or the position that would be the same as if they were not installed.

End of Mem8Plus Construction Notes

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