IOB-1

SERIAL/PARALLEL INTERFACE BOARD

c) 1980, WAMECO INC.

SYSTEM COMPATABILITY

S-100 (Altair, , IMSAI, , etc.) bus compatible.

I/O PORTS

Two parallel I/O ports with full handshaking status.

One port is designated as an output port, the other as an input port.

Each Status or handshake signal polarity can be reversed.

Status of ports may be polled or connected to an interrupt vector, all ports have interrupt capability.

The INTEL₃ 8255A Programmable Peripheral Interface and 8251 Universal Synchronous/Asynchronous Receiver/Transmitter is used.

One serial I/O port with crystal control selectable 110, and 75 to 96 band rate.

The serial port may be used as a 300 baud Kansas City Standard cassette or a communications interface.

The communications interface can be configured as an EIA RS-232, TTL, or 20ma current loop signal.

BOARD ADDRESSING

The I/O ports use six I/O port locations which may be assigned any one of 32 starting location boundries.

1-Trademark of Altair Inc. 2-Trademark of IMS Associates Inc.

3-Trademark of INTEL Inc.

PARTS LIST

2 C28,C39 3 C19,C20,C27 2 C1,C2 31 C3-6,C9-15,C17,C18,C21-25,	QUANTITY	Part Schematic Name	PART TYPE
2 C1, C2			10uf (minimum) 25V (minimum)
2 C1, C2			10uf (minimum) 16V (minimum)
C28-30,C34,C36-38,C40-45			
3	31	C3-6, C9-15, C17, C18, C21-25,	
1 C8 1 C16 2 C31,C33 2 CR1,CR2 3 LN914,IN4148 diode 4 pin connector (APP-923875) 7805,3407-5 +5V regulator 7812,3407-12 +12V regulator 7812,3407-12 +12V regulator 7812,3407-12 +12V regulator 7812,3207-12 -12V regulator 7812,32		C28-30, C34, C36-38, C40-45	0. Ouf 50V ceramic disc capacitor
1 C16 2 C31,C33 2 CR1,CR2 1 N914,114148 diode 1 J1 4 0p in connector (APP-923875) 2 Q1,Q2 7805,340T-5 +5V regulator 7812,340T-12 +12V regulator 7812,340T-12 +12V regulator 7812,320T-12 -12V regulator 7818,00m 4W 5% resistor 782,00m 4W 5% resistor 782,00m		C7, C32, C35	0.01uf 50V ceramic disc capacitor
2 C31,C33 27pf 50V ceramic disc 1N914,1N4148 diode 1 J1 40 pin connector (APP-923875) 7805,340T-5 +5V regulator 7805,340T-12 +12V regulator 7812,340T-12 +12V regulator 7912,320T-12 -12V regulator 79			
CR1 CR2			0.056uf 50V ceramic disc
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Q5			
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	2	U16,U26	V 74L5367

QUANTITY	Part	Schematic	Name	PART	TYPE
1	U18	Same Share			21
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Tools and Supplies Needed for Construction of IOB-1

1 Multimeter

Kadolyan Ber Buraha

- 1 25 Watt fine tip soldering iron
- 1 bottle flux cleaner
- 1 pair needle nose pliers
- 1 XACTO knife
- 1 pair diagonal cutting pliers
- 1 bottle rosin soldering flux
- 1 roll solder (rosin core .031" or .040" diameter)
- 1 roll solder wick
- 1 magnifying glass

A Service Section :

- 1 strong light
- 1 oscilloscope

I. Assemble of IOB-1

- I-1 Before placing any parts on the board, check the board for any hairline shorts (slivers). All boards have been checked at least three times before shipping. Still, it's a good idea to check any board you buy.
- Using a strong light and a magnifying glass, very carefully check all leads on the top of the board (this is the side marked "COMPONENT SIDE"). If any slivers are found, carefully cut and scrape them with an XACTO knife. The underside of the board will be checked after assembly.
- I-3 Place all of the 8,14,16,28 and 40 pin sockets in their positions on the top (component) side of the board.

CAUTION

DO NOT PUT SOCKETS IN THE POSITIONS OF THE FIVE (S1-S5) EIGHT POSITION DIP SWITCHES. THESE SWITCHES MUST NOT BE SOCKETED SINCE THEY WILL NOT STAY IN A SOCKET WHEN THE BOARD IS IN USE.

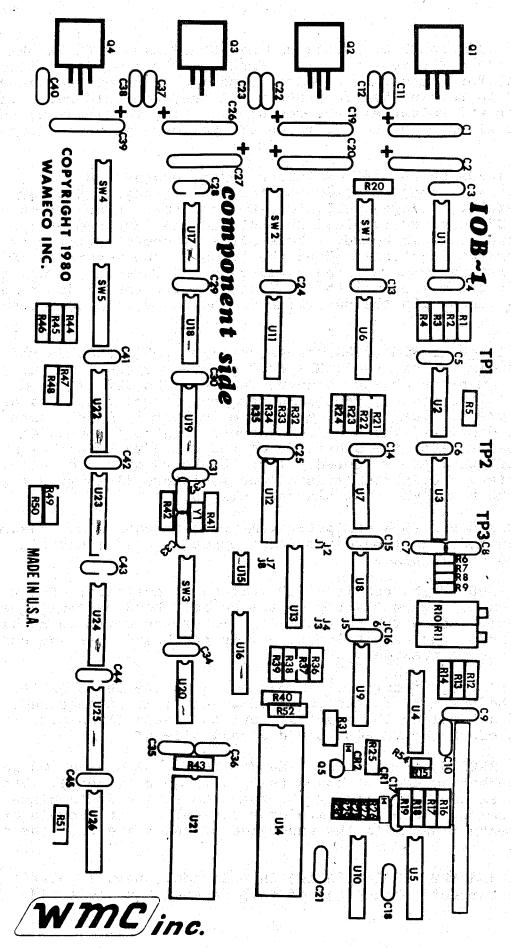


Figure 1. Parts Placement Drawing

- I-5 Bend the leads on R1-5, R9,R14,R20-24,R32-39,R44-48 (2.7K ohm red, violet, red) and place in board. Check part placement drawing (figure 1) for correct locations. Bend the leads on the underside of the board to retain them in place until they are soldered. Turn the board over and solder all the resistors. Clip the leads of the resistors flush with the underside of the board with the diagonal pliers.
- I-6 Bend the leads on R6 (18K ohm brown, gray, orange), R7,R13 (4.7K ohm yellow, violet, red), R8 (22K ohm red, red, orange), R12,R29 (47K ohm yellow, violet, orange), R15,R19 (100 ohm brown, black, brown), R16,R43 (270 ohm red, violet, brown), and R18 (33K ohm orange, orange orange) and place in board. Check parts placement drawing (figure 1) for correct locations. Bend the leads on the underside of the board to retain them in place until they are soldered. Turn the board over and solder all the resistors. Clip the leads of the resistors flush with the underside of the board with the diagonal pliers.
- I-7 Bend the leads on R25 (3.3K orange, orange, red), R26,R30,R51 (1K ohm brown, black, red), R27 (27K ohm red, violet, orange), R28 (10K ohm brown, black, orange), R31,R49,R50,R52 (470 ohm yellow, violet, brown), R40 (1.2K ohm brown, red, red), and R41,R42 (560 ohm green, blue, brown) and place in board. Check parts placement drawing (figure 1) for correct locations. Bend the leads on the resistors on the underside of the board to retain them in place until they are soldered. Turn the board over and solder all the resistors. Clip the leads of the resistors flush with the underside of the board with the diagonal pliers.
- I-8 Place R10 and R11 (50K ohm potentiometers) in position. Ensure screw adjustment is toward top (edge opposite gold fingers) of board. Solder in place.
- I-9 Place SW1-SW5 (eight position DIP switch) in position. Ensure ON position is toward the top of the board. Bend several pins on each end of each switch on the underside of the board to retain them in place until they are soldered. Turn the board over and solder the switches in position.
- . I-10 Place Y1 (4.916 MHz crystal) in place. Bend the leads on the underside of the board to retain it in place until it is soldered. Turn the board and solder the crystal. Cut the leads flush with the underside of the board with the diagonal pliers.
 - I-11 Place Q5 (2N2222) in position. Ensure that flat side of Q5 faces toward the bottom edge of board (side with gold fingers). Bend the leads on the underside of the board to retain it in place until it is soldered. Turn the board over and solder the transistor. Cut the leads flush with the underside of the board with the diagonal pliers.
 - I-12 Place CR1 and CR2 (1N4148/1N914) in position. Ensure polarity of diodes is correct (banded end of each faces toward left side of

- board). Bend the leads on the underside of the board to retain them in place until they are soldered. Turn the board over and solder the diodes. Cut the leads flush with the underside of the board with the diagonal pliers.
- I-13 Place J1 (40 pin connector) in position. Ensure that connector faces toward the top of the board. Holding the connector in place, turn the board over. Rest the connector on a book and push down on the board. Tack the two end pins on each end of the connector. When the connector has been firmly tacked in place finish soldering all the other pins on the connector.
- I-14 Bend the leads of C1,C2,C19,C20,C26,C27,C39 (10uf minimum, Tantalum/electrolytic capacitors) and place in position.

 Ensure polarity of the capacitors is correct (see figure 1).

 Bend the leads on the underside of the board to retain them in place until they are soldered. Turn the board over and rest the ends of the board on two books. Solder the leads and clip them flush with the underside of the board with the diagonal pliers.
- I-15 Bend the leads of C3-6,C9-15,C17,C18,C21-25,C28-30,C34,C36-38,C40-45 (0.1 uf disc) and place in position. Bend the leads on the underside of the board to retain them in place until they are soldered. Turn the board over and rest it on books as before. Solder the leads and clip them flush with the underside of the board with diagonal pliers.

CAUTION CAUTION

CHECK DISC CAPACITORS FOR PROPER VALUE BEFORE
INSERTING IN BOARD. ENSURE 0.01 UF AND 0.1 UF
DISC CAPACITORS ARE NOT INTERCHANGED.

The restauration ent boots

- I-16 Bend the leads of C7,C32,C35 (0.01 uf disc) and place in position.d Bend the leads on the underside of the board to retain them in place until they are soldered. Turn the board over and rest it on books as before. Solder the leads and clip them flush with the underside of the board with the diagonal pliers.
- I-17 Bend the leads of C8 (0.033 uf disc), C16 (0.056 uf disc) and C31,C32 (27pf disc) and place in position. Bend the leads on the underside of the board to retain them in place until they are soldered. Turn the board over and rest it on books as before. Solder the leads and clip them flush with the underside of the board with diagonal pliers.
- I-18 Before installing Q1,Q2,(+5 volt regulator), Q3 (+12 volt regulator), and Q4 (-12 volt regualtor), it is recommended that they be tested for proper operation. Attach the test setup as shown in figure 6 for the positive voltage regulators and as shown in figure 7 for the negative voltage regulator.

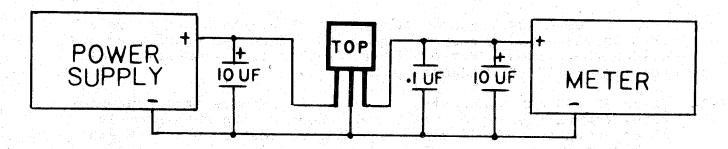


FIGURE 6. TO220 (T PACKAGE) POSITIVE VILTAGE REGULATOR TEST SETUP

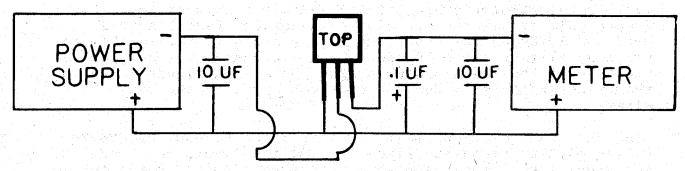


FIGURE 7. TO220 (T PACKAGE) NEGATIVE VOLTAGE REGULATOR TEST SETUP

Place the multimeter in a DC range that will allow a minimum of 5 volts over the regulator voltage being tested to be displayed. The input voltage has to be a minimum 2 volts more positive than the regulated voltage for a posistive regulator and 2 volts more negative for a negative regulator before proper regulation will take place. If the power supply has a voltmeter, observe the input voltage on it during the test. If the power supply does not have a voltmeter, swtich the meter lead between the output and input leads of the regulator during the test. This will allow both voltages to be monitored.

- I-19 Slowly increase the input voltage and observe the output voltage. When the input voltage is between 2.0 and 2.5 volts more positive for positive regulators and more negative for negative regulators than the rated regulator voltage, the regulator should have an output voltage .2 volts of its rated voltage. It is possible that a regulator will be slightly out of tolerance because of no load on the output. If this occurs, attach a 1K ohm ¼W resistor between the output and ground. If the regulator is still out of tolerance reject it. Replace any regulator that does not meet the specified voltage.
- I-20 When the regulators have been tested as outlined above, place the regulators on the board so that the mounting hole on the regulator lines up with the corresponding hole on the IOB-1. Ensure that

each regulator is placed in the proper place (see figure 1). Note where the leads of each regulator pass over the connection holes on the IOB-1. Bend the leads of each regulator so that the leads can be inserted into the proper holes. Mount the regulators on the board with a heatsink between the regulator and the board. Fasten the heatsink and regulator to the board fingertight using a $6-32 \times 3/8$ " machine nut and screw. Solder the leads of the regulators in place.

- I-21 Remove the nuts and screws from the regulators. Bend the regulators upward and remove the heatsinks. Place a moderate amount of silicone thermal compound on the underside of the regulator and heatsink with a Q tip cotton swab. Coat the areas with an evan coating. Reinstall the heatsinks and screw. Install a lock washer on the screw before putting the nut on. Tighten the nuts down securely.
- I-22 Clean off the flux on the board with flux cleaner.
- II Inspection and Testing
- II-1 Use a bright light and magnifying glass to inspect all the traces on the underside of the board. If any slivers are found, cut and scrape them with the XACTO knife. Use the solderwick and soldering iron to remove any solder bridges found. Cover the solder bridge with flux and place a clean piece of solderwick on top of the bridge. Place a soldering iron on top of the solder wick and hold until solder is seen flowing up into the solderwick. Remove the iron and wick. Check to see if the bridge has been completely removed. If not, repeat the process until the bridge has been removed. Clean the flux off the board with flux cleaner.

NOTE

AT THIS TIME NO IC'S HAVE BEEN INSTALLED ON THE BOARD.

DO NOT INSTALL IC'S ON THE BOARD UNTIL CALLED FOR IN
THE CHECKOUT PROCEDURE.

II-2 Place all switches of SW1-SW5 dip switches in the OFF position. Place the multimeter in the R x 1 scale. Place one probe on the gold finger for pin 1. Place the other probe on all the other fingers sequentially to check for shorts. Repeat this procedure for each pin. There should be only two sets of pins that are shorted; 1 to 51 and 50 to 100. If any other pair of pins, use a strong light and magnifying glass to locate the solder bridge or sliver causing the short. When the short has been located, correct it as outlined above in II-1.

WARNING

DO NOT INSTALL OR REMOVE ANY BOARD IN COMPUTER WITH POWER ON. DAMAGE TO BOARDS AND COMPUTER MAY RESULT.

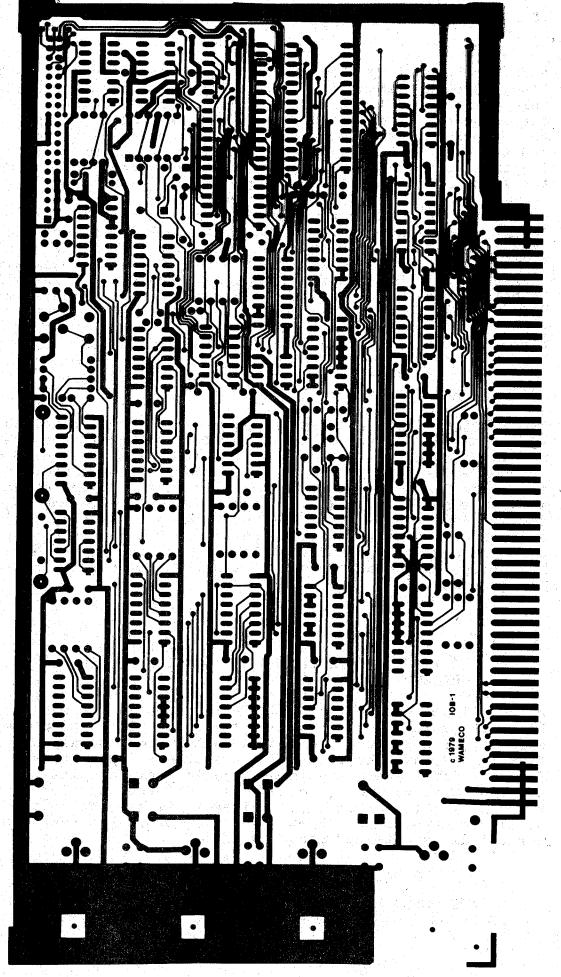


Figure 3. Component Side of IOB-1

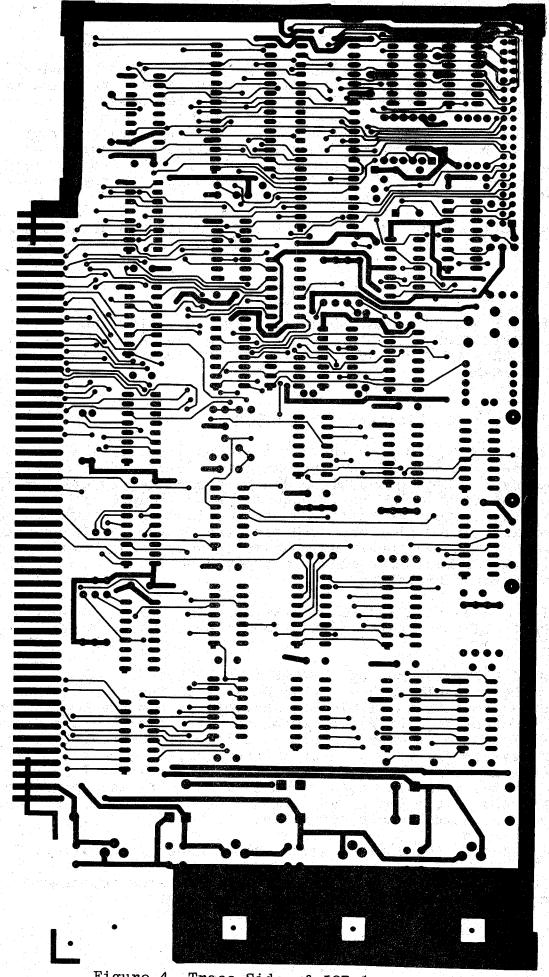


Figure 4. Trace Side of IOB-1

- II-3 Ensure computer is OFF. Plug the IOB-1 into the motherboard. Check that the IOB-1 is correctly plugged in and the board is fully seated in the connector. Turn computer power ON and check the outputs of all four regulators on the IOB-1. If any regulator does not have a correct output, turn computer power OFF and replace the defective regulator. Repeat II-3 untill all regulator voltages are good. If voltages are good, turn computer power OFF and remove the IOB-1 from the motherboard.
- II-4 Install all IC's on the IOB-1. Check the parts placement drawing (see figure 1) for proper location and correct polarity of IC's.

CAUTION

ENSURE ALL IC'S ARE INSTALLED CORRECTLY. INCORRECT POLARIZATION OF AN IC WILL RESULT IN DAMAGE TO THE IC AND WILL CAUSE SUBSEQUENT TROUBLES TO APPEAR ON THE BOARD.

- III Discussion of 8255, 8251 and IOB-1 Design
 - III-1 The 8255 has 24 I/O pins which are broken into two groups of 12. These can be used in three major modes of operation (0,1,2). Mode 0: Each group of 12 can be programmed in sets of four pins to be input or output. Mode 1: Each group of 12 will have eight lines which can be programmed for input or output, three of remaining four pins are used for handshaking and interrupt. Mode 2: A bidirectional bus mode which uses eight lines for a bidirectional bus, five lines (one borrowed from the other group) are used for handshaking.
 - III-2 The IOB-1 uses only Mode 1 operation of the 8255. One port is input eight bit parallel and the other is output eight bit parallel.
- The 8251 USART is used by the CPU as a peripheral device operating with almost any erial data transmission technique. The USART accepts parallel data characters from the CPU and converts converts them to continuous serial output. Serial input from an external source is converted to parallel data for the CPU. The USART signals the CPU whenever it has received a character from the outside or is ready to accept another character from the CPU. USART status including data transmission errors and control signals can be used by the CPU at any time. The 8251 will perform Synchronous or Asynchronous operation.
- III-4 The IOB-1 uses the 8251 in Asynchronous mode of operation.
- III-5 The IOB-1 has five 8 position DIP switches. The assignment of usage for each switch is given in Table A.

SWITCH	USAGE
1,2 3 4 5	Serial I/O Baud Rate Settings I/O and Clock Input Selection Vectored Interrupt Selection I/O Address and Mode Setting Selection

Table A. Switch Usage Assignment

NOTE

ALL SWITCHES ARE CONFIGURED FOR ON = Ø (logic low) OFF = 1 (logic high). SEE FIGURE BELOW.

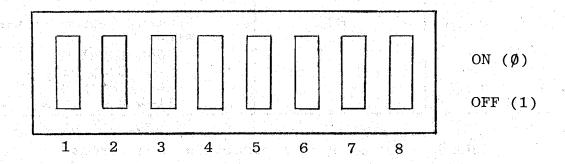


Figure 2. Switch Layout

III-6 The 8251 is used in the IOB-1 as an Asynchronous serial port controller. There are three words that the 8251 uses: The Mode Instruction word, the Command Instruction word and the Status Read word. Two are output to the 8251 by the CPU, the other is requested by the CPU from the 8251.

FORMAT: Mode Instruction - Sent by CPU as first word after internal reset. Determines functional definition of 8251.

FC		P	PC		Ĺ.	BRF		
D 7	D6	D5	D4	D3	D2	D1	DØ	

BITS AFFECTED	FIELD	EXPLANATION
DØ, D1	BRF	Baud Rate Factor ØØ=SYN mode (illegal for IOB-1) Ø1=ASYN X 1 1Ø=ASYN X 16 (use this for IOB-1 11=ASYN X 64
D2, D3	CL	Character Length \$\phi \text{0}=5 \text{ Bits} \\ \$\phi 1=6 \text{ Bits} \\ \$1\$\phi=7 \text{ Bits} \text{ (normal ASCII)} \\ \$11=8 \text{ Bits}
D4, D5	PC	Parity Control ØØ=No Parity Ø1=Odd Parity 1Ø=No Parity 11=Even Parity
D6, D7	FC	Framing Control (number of Stop Bits) ØØ=Not Valid Ø1=1 Stop Bit 1Ø=1½ Stop Bits 11=2 Stop Bits

TABLE B. Serial Mode Instruction Word Format

FORMAT: Command Instruction - Sent by CPU as second word after internal reset. Controls actual operation of the selected format.

					The state of	in the second second			
	EH	IR	RTS	ER	SBRK	RxE	DTR	TxEN	
- 1									
	D7	D 6	D5	D4	D3	D 2	D1	DØ	ŀ

BITS AFFECTED	FIELD	EXPLANATION
DØ	TxEN	Transmit Enable Ø=Enable 1=Disable
D1	DTR	Data Terminal Relay 1=Forces DTR Output to Zero
D2	RxE	Receive Enable Ø=Enable 1=Disable

	BITS AFFECTED	FIELD	EXPLANATION
		S. S	
	D3	SBRK	Send Break Character
			Ø=Normal Operation
	la de Perro do Espaina (Perroque III). Orași especial de Laboratea (Espaina)		1=Forces TxD "Low"
	D4	ER	Error Reset
		Pelan de Mig	1=Reset Error Flags PF,OE,FE
			(see Status Read definitions)
	D5	RTS	Request To Send
			1=Forces RTS Output to Zero
	D6	T.D	
		${ m IR}$	Internal Reset 1=Returns 8251 to Mode Instruction
			Format
	$\mathbf{D7}_{7}$, which is the state of $\mathbf{D7}_{7}$	EH	Enter Hunt Mode
4.3	格 建净效 紧张 多数自由的结	District Control of the State of	Ø=Used for IOB-1
	医施克特氏病 医克里特氏病		1=Enable Search for Synch Characters
	Laran a sina de nade najari di		(Illegal for IOB-1)

TABLE C. Serial Command Instruction Word Format

FORMAT: Status Read - Sent by 8251 upon request by CPU (see Port 6 on SW5). Gives Status of the device to ascertain if errors have occured or other condition that requires the processors attention.

BITS AFFECTED	FIELD	EXPLANATION
DØ	TxRDY	Transmitter Relay - This flag indicates that the 8251 is ready to receive a Data Character or command. The flag can only be asserted if TxEN is set. TxRDY is
		reset when the 8251 receives the character from the CPU.
D1	RxRDY	Receiver Ready - This flag indicates that the 8251 has received a character on its serial input and is ready to transfer it
		to the system CPU. The flag can only be asserted if RxE is set. RxRDY is reset when the character is read by the CPU.
D2	TxE	Transmitter Empty - This flag is set when the parallel to serial converter is empty (Data has been sent).

BITS AFFECTED	FIELD	EXPLANATION
D3	PE OE	Parity Error - This flag is set when a parity error has been detected by the 8251. PE will not inhibit operation of the 8251. This bit is reset by the command instruction bit ER. Overrun Error - This flag is set when the system CPU does not read a character before the next one becomes available to the 8251. OE does not inhibit the operation of the 8251, but the overrun (older) bit is lost. This bit is reset by the command instruction bit ER.
D5	FE	Framing Error - This flag is set when a valid stop bit is not detected at the end of every character. FE does not inhibit the operation of the 8251. This bit is reset by the command instruction bit ER.
D6	SYNDET	Synch Detect - Used in synchronous mode only. Does not apply to IOB-1.
D7	DSR	Data Set Relay - A general purpose input signal which can be read by the system computer. It indicates that the DSR is at a zero level.

TABLE D. Serial Status Read Format

There are three switches used with the 8251: SW1, SW2 and SW3. SW1 and SW2 are used to select the serial I/O baud rate (see Table E). SW3 is used to select the type of interface (RS-232, TTL, Current Loop or Cassette) that is required by the selected peripheral (see Table F).

Baud Rate	SW1	4 5	6 7,8	1 2	3	W2	5	6	7	8
					4.6					
75	N on	on on	on N	on on	on,	on	on	on	on	on
110	O off	on off	on O	off on	on	on	on	on ·	off	off
150	T on	on on	off T	on on	on	on .	on	on	on	off
300	on	on off	off	on on	on	on	on	on	on	off
600	U on	off off	off U	on on	on	on	on	on	on	off
1200	S off	off off	off S	on on	on	on	on	on	on	off
2400	E off	off off	off E	on on	on	off	on	on	on	off
4800	D off	off off	off D	on on	off	off	on	on	on	off
9600	off	off off	off	on off	off	off	on	on	on	off
		W 1995								

TABLE E. Serial I/O Baud Rate Switch Settings

ALL SWITCHES ARE CONFIGURED FOR ON = Ø (LOGIC LOW) OFF = 1 (LOGIC HIGH). SEE FIGURE 2.

USAGE	C	/C	TOI				NOT USED		
Switch #	1	2	3	4	5	6	7	8	

SWITCH	#	USAGE	EXPLANATION
1,2		C/C	Communication/Cassette
	***		$\emptyset 1$ = All Synch communication except cassette $1\emptyset$ = Cassette Operation
3-6		TOI	Type of Interface 1110 = RS-232 1101 = Current Loop
			1Ø11 = TTL Ø111 = Cassette

TABLE F. Serial Type of Interface

NOTE

FOR CASSETTE OPERATION, 300 BAUD SHOULD BE SELECTED ON SW1 AND SW2. THERE ARE NO RESTRICTIONS ON CLOCK RATEWFOR ANY OTHER SERIAL COMMUNICATION.

III-8 The peripheral connector (J1) should have the type of interface desired connected to the pins as shown in Table G.

TYPE OF INTERFACE	DESIRED	J1 PINS
		input output
RS-232		5,6 7,8
Current Loop		13,14 15,16
TTL Cassette		$egin{array}{cccccccccccccccccccccccccccccccccccc$

TABLE G. J1 Desired Interface Connections

III-9 The 8255 is used in the IOB-1 as a dual eight bit parallel port controller. One port (port A) is used as an output port, a second port (port B) is used as an input port. A third port (port C) is used for handshaking and status for ports A and B. The 8255 uses an eight bit mode controll word to program its mode selections, A and B port definitions and C port setup (see Table H). Any of the eight bits of port C can be Set or Reset using a single Output instruction to that port's address using the Bit Set/Reset format shown in Table I. The status register of the 8255 can be read at any time by performing a Read operation of the C port address. The meanings of the status bits are shown in Table J.

FORMAT: Mode control word - sent by CPU determines functional definition of 8255.

Ì	MSF	MSA	PA	PCA	MSB	PB	PCB
	D 7	D6 D5	D4	D3	D 2	D1	DØ

BITS AFFECTED	FIELD	EXPLANATION
DØ	PCB	Port C (lower) Group B Ø = Output 1 = Input - used for IOB-1
D1	PB	Port B Ø = Output 1 = Input - used for IOB-1
D2	MSB	Mode Selection Group B $\emptyset = \text{Mode } \emptyset$ $1 = \text{Mode } 1 - \text{used for IOB-1}$
D3	PCA	Port C (upper) Group A Ø = Output - used for IOB-1 1 = Input
D4	PA	Port A Ø = Output - used for IOB-1 1 = Input
D5,D6	MSA	Mode Selection Group A $\emptyset\emptyset$ = Mode \emptyset $\emptyset1$ = Mode 1 - used for IOB-1 $1X$ = Mode 2
D7	MSF	Mode Set Flag Ø = Inactive 1 = Active - used for IOB-1

NOTE

AS SHOWN ABOVE, THE CONTROLL WORD FOR THE IOB-1 IS 10100111.

FORMAT: Set/Reset Word - any status of flag bit may be individually Set or Reset by sending a mode controll word with the data bit D7 set to Ø.

3	СВ	Ø	Ø	Ø	PB	SB
	D 7	D6	D5	D4	D 3 D 2 D 1	/ D ø

BITS AFFECTED	FIELD	EXPLANATION
DØ	SB	Selection of Bit Value Ø = Set Selected Bit to Zero 1 = Set Selected Bit to One
D1,D2,D3	PB	Bit to be Programmed $\emptyset \emptyset \emptyset = \text{Bit } \emptyset$ $\emptyset \emptyset 1 = \text{Bit } 1 (\text{IOB-1 } \overline{\text{IBF}}_B)$ $\emptyset 1\emptyset = \text{Bit } 2 (\text{IOB-1 } \overline{\text{STB}}_B)$ $\emptyset 11 = \text{Bit } 3$ $1\emptyset \emptyset = \text{Bit } 4$ $1\emptyset 1 = \text{Bit } 5$ $11\emptyset = \text{Bit } 6 (\text{IOB-1 } \overline{\text{ACK}}_A)$ $111 = \text{Bit } 7 (\text{IOB-1 } \overline{\text{OBF}}_A)$
D4,D5,D6	Ø ØØ CB	For IOB-1 usage this filed must be set to all Zeros Set/Reset Bit Selection - this bit
		must be set to zero to enable Set/Reset bit selection

TABLE I. Parallel Set/Reset Bit Word Format

FORMAT: Parallel Status Read - sent by 8255 when address read instruction is made by CPU. The address read will be the selectable address boundry + 101 (see Table J).

BITS AFFECTED	USAGE	EXPLANATION JUMPER TO USE TO INVE			
DØ	×	Don't care, not used			
D1	IBF _B	This line is sent to an external device to acknowledge the fact that data has been received by the 8255. It is an active high signal. It is reset as soon as the CPU (8080) has read the data from the 8255.	5,6		
D2	$\overline{\mathtt{STB}}_{\mathrm{B}}$	This line is used by an external device to strobe data into the input port of the 8255. This is an active low signal.	1,2		
D3,4,5	x	Don't care, not used			
D6	ACK _A	This line is sent from a peripheral device to acknowledge the fact that it has taken the data from 8255. This is an active low signal It also Resets $\overline{\text{OBF}}_{A}$.			
		This line is sent to an external device to indicate that the CPU (8080) has loaded data to the 8255 and is available. This is an active low signal and is set by a CPU output to the 8255 data out port. It is set by ACK A	7,8		

TABLE J. Parallel Status Read Word Format

III-10 The IOB-1 has the capability of two different vectored interrupt priorities being assigned to each series and parallel port. If no vectored capability is desired, all switches on SW4 would be placed OFF. If no PINT is desired (polled interrupt is desired), lift pin 13 of U16 or pin 6 of U18. The IOB-1 will then not generate an interrupt but the board can be polled to see if any data has been received.

USAGE	S07	S06	SI5	S14	PA03	PA02	PBI1	PBIØ	1.132
SWITCH #	1	2	3	4	5	6	7	8	

SWITCH #	USAGE	EXPLANATION
1 2 3 4 5 6 7 8	S07 S06 S15 S14 PA03 PA02 PB11 PB10	Serial Output - Priority Seven Serial Output - Priority Six Serial Input - Priority Five Serial Input - Priority Four Parallel Output Port A - Priority three Parallel Output Port A - Priority two Parallel Input Port B - Priority one Parallel Input Port B - Priority zero
		NOTE Each dual priority selection for a particular input or output type (I.E.: S07,S06,SI5,SI4,PA03,PA02,PBI1,PB10) is tied together on the board side of SW4 (see Figure 5, IOB-1 Schematic). Only one priority should be assigned to each type input or output since the board cannot tell the difference.

TABLE K. Priority Interrupt Assignment Table for SW4

ADDRESS BIT	NOT USED		A11	A12	A13	A14	A15	
SWITCH	1 2	3	4	5	6	7	8	

SWITCH #	ADDRESS BIT	EXPLANATION
4-8	A11-A15	Selectable Address Boundry - This allows for any one of 32 boundries to be selected. Each boundry is the starting address location of eight addresses, six of which are used.
	A1Ø-A8	Selectable Mode Address - This allows the selection of the address location of the mode type (data or status) for I/O usage.

SWITCH #	ADDRESS BIT	EXPLANATION
		<pre>\$\psi \phi = \text{ parallel data port A; data out} \$\phi 01 = \text{ parallel data port B; data in} \$\phi 10 = \text{ parallel data ports A and B;} \$\text{ status on input} \$\text{ set flags on output} \$\phi 11 = \text{ Parallel data ports A and B;} \$\text{ mode control on output} \$100 = \text{ serial data port; data in and out} \$101 = \text{ serial data port;} \$\text{ status on input} \$\text{ control on output} \$110 = \text{ not used} \$111 = \text{ not used} \$\text{ 111 = not used} \$ \text{ port A; data in and out} \$ \text{ status on input} \$\text{ control on output} \$ \text{ output} \$ \text{ output} \$ \text{ output} \$ </pre>

TABLE L. I/O Address And Mode Setting Selection SW5

IV CASSETTE TIMING SETUP

- IV-1 For proper operation of the Kansas City Standard Interface, two pots (R10 and r11) must be adjusted.
- IV-2 Configure the IOB-1 for 300 band cassette operation.
- IV-3 Output to the cassette for 10 to 15 minutes the letter uppercase U (ASCII code 55 Hex).
- IV-4 Input the cassette data just recorded (letter U) and adjust R10 and R11 for the correct waveforms.

TEST POINT	DATA BEING MONITORED	CORRECT INDICATION	ADJUSTMENT TO BE MADE
TP1 TP2 TP3	Cassette Data (Letter U) 600Hz Square Wave, TTL level 4800Hz Square Wave,	Steady Signal Steady Signal	none Adjust R11 until signal is steady
	TTL level	proper frequency and symmetrical waveform	Adjust R1Ø

TABLE M. Cassette Pot Adjustments

ENGINEERING NOTES

The IOB-1 parallel ports are configured normally as a single output and single input port with the proper "handshaking" signals. However, additional configurations are possible b at the inconvenience of missing handshake and status signals. The impact of the missing signals may be minimized through judicious programming of the 8255A. The following data lists the possible combinations of input/output configurations:

Port A	Port B	Port C	Comment
Output	Input	Status & STB: for both A&B	Normal configuration of IOB-1. Control Port Data = A6
Output	Output	Stat <u>us & STB:</u> Use \overrightarrow{OBF}_A , \overrightarrow{ACK}_A	16 Bit output transfer output Port "B" first then Port "A". Control Port Data = AØ.
Input	Input	$\frac{\text{Status & STB:}}{\text{use STB}_{B}}, \frac{\text{STB:}}{\text{IBF}_{B}}$	16 bit input transfer input Port "A" first then Port "B". Control Port Data = B6

The above data is valid for Mode 1 operation of the INTEL 8255A with port "C" not being used. It should be noted that there is only one set of handshake signals available when ports "A" and "B" are configured as both output or both input ports.

ENGINEERING NOTES

The following programs are test routines to verify the proper operation at the IOB-1 data ports. The programs assume that a front panel with port "FF" input/output port is available. Also, switches 4,5,6,7, and 8 are "CLOSED" on SW5.

Location	<u>Data</u>	Assembler	<u>Comment</u>
00 01 02 03 04 05 06 07 08 09 A	3E A6 D3 Ø3 DB FF D3 Ø9 C3 Ø4	MVI, A MODE OUT Control port IN Front Panel OUT Port "A" JMP Lower Upper	;This routine teste the output; of the 8255A. Testing is ac-; complished by toggling data; switches A8 through A15 and; observing the appropriate; output line changing state; with an oscilloscope or; voltmeter. The lines tested are; OUT Ø through OUT 7.
Location	<u>Data</u>	Assembler	<u>Comment</u>
00 01 02 03 04 05 06 07 08	3E A6 D3 Ø3 DB Ø1 D3 FF C3 Ø4	MVI,A MODE OUT Contrl Port IN Port "B" OUT Front Panel JMP Lower	;This routine tests the input ;of the 8255A. Testing is ac-;complished by connecting a ;TTL signal to data lines ;IN Ø through IN 7. By changing the ;input to a high or low signal ;the appropriate data bit should ;toggle on the front panel ;display port (FF _H).
A	ØØ	Upper	

Cassette Alignment Procedure

- 1. Place the IOB-1 on an extender board. Insure that the board is properly aligned to the mating extender board connector.
- 2. Input a 100mv (RMS) sinewave (or squarewave), 2400HZ, on Pin 1 of the I/O connector at the top right-hand side of the IOB-1. Don't forget to connect a ground to pin 2.
- 3. Adjust pot R11 until the signal at U9 pin 6 compares to the signal of U9 pin 5 as shown in figure 1.
- 4. Adjust pot R10 until the signal at TP3 compares to the signal at TP2 as shown in figure 1.

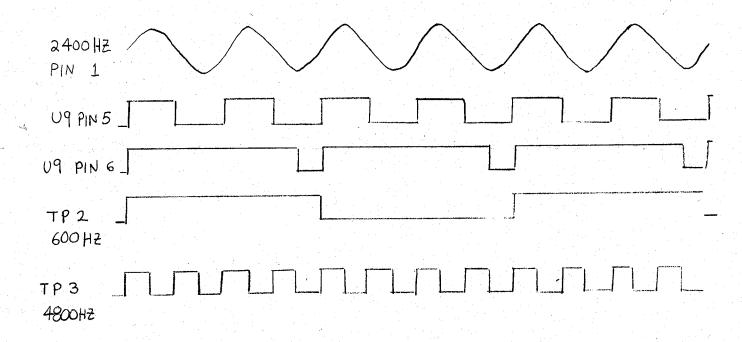
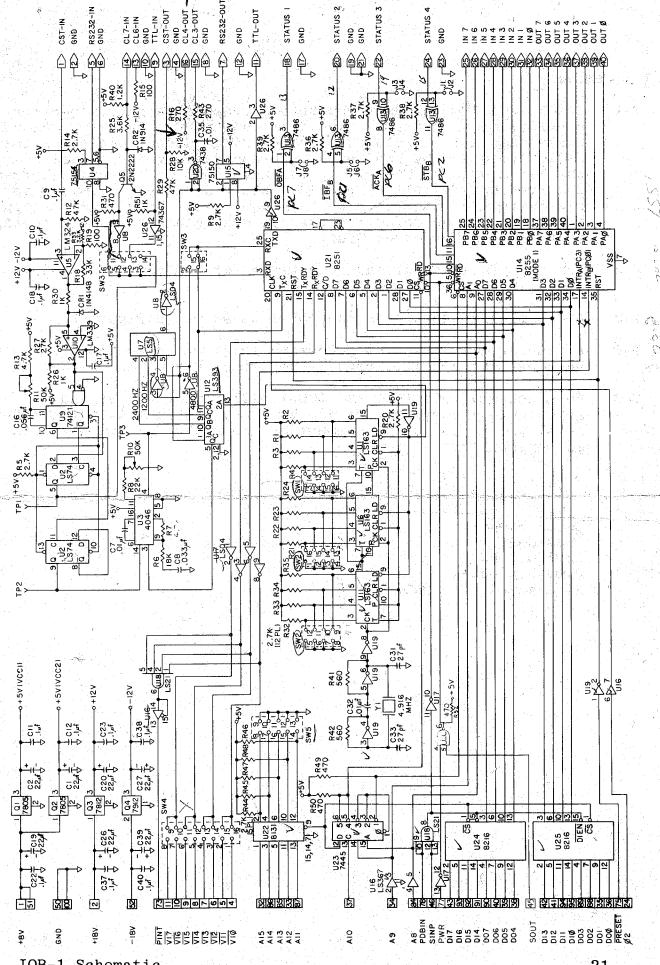


FIGURE 1

5. It may be necessary to readjust R10 slightly until there are no errors during data input from a cassette.

IOB-1 ERRATA

- 1. R54 on the soldermask is R53 in the parts list and schematic.
- 2. R17 is not used.
- 3. An extra inverter was added on the CL7 input, therefore U8 8,9 inverter must be jumpered out. This may be done by cutting the trace coming out of U8 pin 8 and adding a jumper between U8 pin 9 and SW3 pin 11.
- R16 was inadvertently connected to -12V rather than +12V. This may be corrected easiest by putting R16 in so that the left side is in R16's left side (side close to U4) and the right side is in the right side of R17 (side close to U5). Then jumper the right side of R16 (that now is in U17's right side) to the +12V (pin 4 of U5).



IOB-1 Schematic

V General

- V-1 The WAMECO INC. product you have purchased is guaranteed for a period of ninety (90) days from date of purchase from your dealer against defects in manufacturing. Upon receipt of the defective board by WAMECO INC., prepaid freight or mailing, the board will be cheerfully replaced and the shipping charges incurred by you will be repaid. the guarantee is limited to replacement of the board with an equivalent board even though the board may be defective through negligence in manufacturing or through other other fault.
- V-2 For reference, front and rear trace layouts for the IOB-1 is shown in Figures 3 and 4.
- V-3 A detailed schematic of the IOB-1 is shown in Figure 5.
- V-4 A general discussion on soldering is given in Appendix A. We hope that you will read it before constructing the IOB-1.
- V-5 We sincerely hope that the IOB-1 will give you long and satisfactory service. If you have any problems with the IOB-1, or if you just want to comment on the board, please write to me personally.

Chuck Naegeli President WAMECO, INC. P.O. Box 855 El Granada, CA 94018