VECTOR

8"

FLOPPY DISK CONTROLLER

Technical Information

VECTOR 8" FLOPPY DISK CONTROLLER BOARD

Revision 1

TECHNICAL INFORMATION MANUAL

REVISION A

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FOREWORD

Audience	This manual is intended for dealers, user's, and service personnel with a moderate knowledge of microcomputers.
Scope	It describes what the Vector 8" Floppy Disk Controller Board does, and how to test and adjust the board.
Organization	Each section is written at a uniform level of technical depth. "User's Information Sheet" tells the user how the board is addressed and the specifications, "Perspective" gives a general description of the board, "User's Guide" tells how to format the disks, "Theory of Operation" explains the circuitry of the board, and "Tests and Adjustments" explain testing and alignment procedures.

USER'S INFORMATION SHEET

Port Addresses used by the 8" Floppy Disk Controller Board

The controller board is shipped with the following port addresses preselected for the signals listed.

Port	Input	Output
E0	Status	Command
E1	Track	Track
E2	Sector	Data
E3	Data	Data
E4	DRQ Status	Drive, Side, Double density select
E5	DRQ Wait	
E6	Serial Data	Serial Data
E7	Serial Status	Serial command

Ports E0 thru E5 are located on the 1793 chip. Ports E6 and E7 are located on the 8251 chip (refer to Intel 8080 user's manual). In order to use standard Vector Graphic software, the board must remain addressed as is.

Synchronous:

Rates - DC-56K

Synch detect - Can be wired for internal or external synch.
8251 SYNDET line is not connected.

Clock - Not now connected to the external world as required for synchronous operation

Parity - Even, odd, or none, programmable

Data bits - 5 to 8, programmable

Synch character - single or double synch character can be programmed

Specifications - Floppy Disk Controller

Data Transfer Rate - Single Density: 250K bits/sec

Data Transfer Rate - Double Density: 500K bits/sec

Diskette Format - Single Density: IBM 3740

Diskette Format - Double density: IBM System 34

Controller Port Addresses - E0H to E5H

Electrical Characteristics - 1793 IC

Maximum Ratings:

Vdd with respect to Vss (ground) = 15 to 0.3V

Max. voltage to any input with respect to Vss = 15 to 0.3V

Operating Temperature	0 C to 70 C
Storage Temperature	-55 C to +125 C

Specifications - Serial Port

Serial Port - 1, using 8251 controller chip

Port Addresses - E6H and E7H

Signal Levels - EIA RS-232C

RS-232 handshaking - RXD, TXD, and DSR are currently wired. CTS goes to ground.

Asynchronous:

Rates - 110-9600 baud (switch selectable)

Data bits - 5 to 8, programmable

Stop bits - 1, 1 1/2, or 2, programmable

Parity - Even, odd, or none, programmable

Internal Clock - 1, 16, 64, programmable

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I. Perspective

1.1 General Description

The Vector Graphic 8" Floppy Disk Controller Board is a versatile single and double density floppy disk controller implemented on a 5-by-10 inch PCBA that plugs into the S-100 bus.

The heart of the board is the 1793 Floppy Disk Formatter/Controller IC. The 1793 is a MOS LSI device that performs the function of a floppy disk formatter/controller in a single chip implement.

The board is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM).

The board contains all the necessary features to read/write and format a double density diskette. These features include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the board design was made as close as possible with the computer interface, instruction set and I/O registers being identical. Also, head load control is identical.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers.

The board also contains one serial RS-232 I/O port that is available to the user.

The heart of the serial I/O port is the 8251 USART integrated circuit. On-board circuitry allows the user to choose a serial transmission speed between 110 baud and 9600 baud controlled by an on-board baud rate generator. Provisions are also available for the speed to be controlled by an external clock. Jumper areas have been provided to allow the user to choose whether the serial port will be configured as DCE or DTE.

II. User's Guide

2.1 Formatting the Disk

Formatting the disk is a relatively simple task when operating programmed I/O or operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the 1793 raises the Data Request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the 1793 detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, in FM an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

2.1.1 IBM 3740 Format

Disks may be formatted in IBM 3740 single density with sector lengths of 128 bytes. In order to format a diskette, the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FFH
6	00H
1	FCH (Index Mark)
26*	FFH
6	00H
1	FEH (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00H
1	F7H (2CRC's written)
11	FFH
6	00H
1	FBH (Data Address Mark)
128	Data (IBM uses E5)
1	F7H (2 CRC's written)
27	FFH
247**	FFH

*Write bracketed field 26 times
**Continue writing until 1793 interrupts out.
Approx. 247 bytes.

2.1.2 IBM System 34 Format

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette, the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
80	4EH
12	00H
3	F6H
1	FCH (Index Mark)
50*	4EH
12	00H
3	F5H
1	FEH (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 thru 1)
1	Sector Number (1 thru 1A)
1	01H
1	F7H (2 CRC's written)
22	4EH
12	00H
3	F5H
1	FBH (data Address Mark)
256	Data
1	F7H (2 CRC's written)
54	4EH
598**	4EH

*Write bracketed field 26 times

**Continued writing until 1793 interrupts out.
Approx. 598 bytes.

2.2 Board Addressing

The board occupies 8 ports beginning at the base address up to base address +7. Base address is the lowest address assigned to the board. The base address of the board can be determined by soldering the jumpers in area E as follows:

Address	Jumper
00H	2-6,3-8,1-4
20H	2-6,3-8,1-5
40H	2-6,3-8,1-4
60H	2-6,3-9,1-5
80H	2-7,3-8,1-5
A0H	2-7,3-8,1-5
C0H	2-7,3-9,1-5
E0H	2-7,3-9,1-5

2.3 Serial I/O Port

A serial I/O port is included in the 8" Floppy Disk Controller Board which allows the user to connect a modem to his standard system without having to disturb the serial port on the ZCB board. This RS-232C port is factory configured as Data terminal Equipment (DTE) so a modem may be connected directly without having to change the signal lines.

If you wish to connect a serial printer or a terminal to this port, area C must be rejumpered as Data Communication Equipment (DCE). Use the DCE column in the following chart. The DTE column shows standard jumpering.

I/O Port Signal Line Jumpering

Signal	DTE	DCE
RxD	5-11	5-17
TxD	6-18	6-17

Four RS-232C handshaking lines are provided for on this board. They may be connected or not as required. The standard jumpering holds DTR (line 20) and RTS (line 4) high on the RS-232C line. CTS (pin 17 on the 8251) is held low. DSR (line 6) is connected through a 1489 buffer to pin 22 of the 8251.

Any or all of the signal or data lines may be changed according to the application. Jumper area D determines which direction the signals are going, i.e., will the port be configured as DTE or DCE.

The port comes configured as DTE which allows it to be connected to a modem. To use this port with a printer, for instance, it must be reconfigured as DCE. To do this, rejumper area C as per the chart below.

Line	DTE	DCE
DTR	3-15	3-9
DSR	4-10	4-16
RTS	1-13	1-7
CTS	2-8	2-14
RxD	5-11	5-17
TxD	6-18	6-12

Jumper area D determines whether there will be a connection between the RS-232C line and the 8251 or not. This is an added option of grounding either side of the connection at jumper area D.

NOTE:A "/" after a signal designation means that the signal is low, e.g., DTR/ is low.

Jumper Area D Standard Configuration

Signal	Pin	Effect
DTR/	5-15	Brings DTR (20) high on RS-232C side
DSR/	3-9	Connects RS-232C to 8251 (22)
RTS/	6-16	Brings RTS (21) high on RS-232C side
CTS/	13-17	Brings CTS (17) low on 8251 side

To change jumper area D consult the board schematic to determine what changes will be required.

For a more detailed discussion of RS-232C and serial communications, consult the ZCB board manual which comes with your system.

2.3.1 Serial Port Address

The address of the serial port can be determined by the base address of the Floppy Disk Controller Board +6 and +7. Other than this, there is no connection between the serial port and the disk controller board.

2.3.2 Baud Rate Select Switch

The rate of serial transmission and reception can be determined by the Baud Rate Select switch located on the upper left-hand side of the board. The switch contains eight rockers labeled "1" to "8" and also labeled "9600," "4800," "2400," "1200," "600," "300," "150," and "110." To select one of the labeled baud rates, press the desired rocker down on the right side labeled "ON" on the end of the chip. Then press all the other rockers toward the "OFF" designation. The result will be that on of the rockers is down toward the right, while the others are down toward the left. Otherwise the serial port will not work. If you are not using the serial port, all the switches should be in the "OFF" position.

2.3.3 Jumper Area A

You can enable the serial port to communicate in the synchronous mode but modifications to the board will be required to accomplish this. Standard jumpering in jumper area A selects the BAUD RATE SELECT switch. An external clock, as required for synchronous operation, can be selected by cutting the standard jumpers between pads 3, 4, and 5, and soldering jumpers between pads 4 and 1, and between 5 and 2.

RS-232C name	Source	RS-232C pin number (at the DB-25)	FDC pin number on 24-pin socket J2	Component connected to on the board	8251 pin name, or other if relevant
Protective Ground	Both	1	24	GND	GND
Transmitted Data	DTE	2	23	JC-6	RxD
Received Data	DCE	3	22	JC-5	TxD
Request to Send	DTE	4	21	JC-1	+12
Clear to Send	DCE	5	20	JC-2	—
Data Set Ready	DCE	6	19	JC-4	DSR/
Signal Ground	Both	7	18	GND	GND
Received Line Signal Detector	DCE	8	17	•	+12
(Reserved for Data Set Testing)	—	9	16	•	—
(Reserved for Data Set Testing)	—	10	15	•	—
(Unassigned)	—	11	14	•	—
Secondary Received Line Signal Det.	DCE	12	13	•	—
Secondary Clear to Send	DCE	13	—	•	—
Secondary Transmitted Data	DTE	14	1	•	—
Transmitter Signal Element Timing (DTE Source)	DTE	15	2	U41-4	—
Secondary Received Data	DCE	16	3	•	—
Receiver Signal Element Timing (DCE Source)	DCE	17	4	U41-10	—
(Unassigned)	—	18	5	•	—
Secondary Request to Send	DTE	19	6	•	—
Data Terminal Ready	DTE	20	7	JC-3	+12
Signal Quality Detector	DCE	21	8	•	—
Ring Indicator	DCE	22	9	•	—
Data Signal rate Detector	Either	23	10	•	—
Transmitter Signal Element Timing (DCE Source)	DCE	24	11	•	—
(Unassigned)	—	25	12	•	—

RS-232C and Connections on 8" Floppy Disk Controller Board

• indicates pad available at 24 pin socket J-2.

III. Theory of Operation

NOTE: a "/" after a signal designation in the text means that signal is inverted (e.g.,"DDEN" is not inverted,"DDEN/" is inverted).

As a supplement to the theory of operation see schematic drawing and the block diagrams shown in figures 3-1 and 3-2. A description of the various circuits on the Disk Controller board are discussed below.

3.1 Power Supply Section

The Disk Controller Board requires +5 Volts, +12 Volts, -5 Volts, and -12 Volts. These are provided by on-board voltage regulators driven from unregulated DC voltages of the S-100 bus. These voltages are filtered by a series of 4.7 uF capacitors.

A 7805 regulator provides the +5 Volts, a 7812 the +12 Volts, a 79L05 the -5 Volts, and a 7912 the -12 Volts.

3.2 Address Decoding

U32, U21, and IC U7 make up the Address Decode Circuit. Jumper area E selects 3 high order bits of the address so the board can be jumpered for a base address of E0H. E6H - E7H select the 8251 USART and E0H - E3H select the 1793 Formatter/Controller.

3.3 RS-232C Drivers

Jumper areas C and D on the schematic can be used to select the board for either DTE (Data Terminal Equipment) or DCE (Data Communication Equipment) via RS-232C handshaking lines.

In order to control an RS-232C handshaking line from the 8251, a signal must pass from an 8251 output pin to the input of one of the driver circuits in a 1488 quad-line driver, using the pads in jumper area D. It must then pass from the output of the 1488, where it is inverted, to the RS-232C line, using the pads in jumper area C.

To respond to an incoming RS-232C handshaking line, the signal must pass through the pads in jumper area C to the input of one of the receiver circuits in a 1489 quad-line receiver. It must then pass from the output of the 1489, where it is inverted, through the pads in jumper area D, to one of the input pins of the 8251.

3.4 VCO and Data Separator

The VCO (Voltage Control Oscillator U27, U28) takes raw data from the disk and synchronizes the Read Clock (Pin 26, U12 on schematic) to data.

3.5 Clock Generator

The Clock Generator provides an 8 MHz clock to the Write Precompensation Circuit and a 2 MHz clock to the Controller.

3.6 Write Precompensation

The data written to the diskette is compensated during the write operation. This is called precompensation. This means that certain data patterns will be shifted slightly reducing the margin for error in the read process. This shift is due to the magnetic recording process. The Shift Register U38 receives a 2 MHz pulse from the clock Generator which is clocked by the same clock that operates U12. U39 is a multiplexer which selects the appropriate bit time in the shift register according to the output from the clock generator. The output of U39 is sent to the disk drive where it is recorded on the diskette.

3.7 Drive Select Decoder

The Drive Select Decoder takes data bits from the S-100 bus and decodes two of them into the 4 drive select lines. Bits 0 and 1 are decoded as the 4 Drive Select lines, bit 2 selects the side of the disk, and bit 3 selects double density enable.

3.8 Programmable Communication Interface - 8251 Chip

The 8251 is a Universal Synchronous/Asynchronus Receiver/Transmitter (USART) chip. The USART accepts data characters from the CPU in parallel form and converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. EIA RS-232C line drivers and receivers interface the RxD and TxD output of the 8251 to the outside world. Discrete components are used to interface with 20 mA teletype signals.

3.9 Disk Formatter and Controller - 1793 Chip

The heart of the Disk Controller Board is the 1793 Floppy Disk Formatter/Controller IC. A general description of this device can be found in Section I of this manual. A Block Diagram of the 1793 can be found in Figure 3-2.

NOTE:

In the following discussion DAL refers to the 8 data access lines. See 3.9.1 for more details.

Data Shift Register

This 8-bit register assembles serial data from the Read Data input (RAW

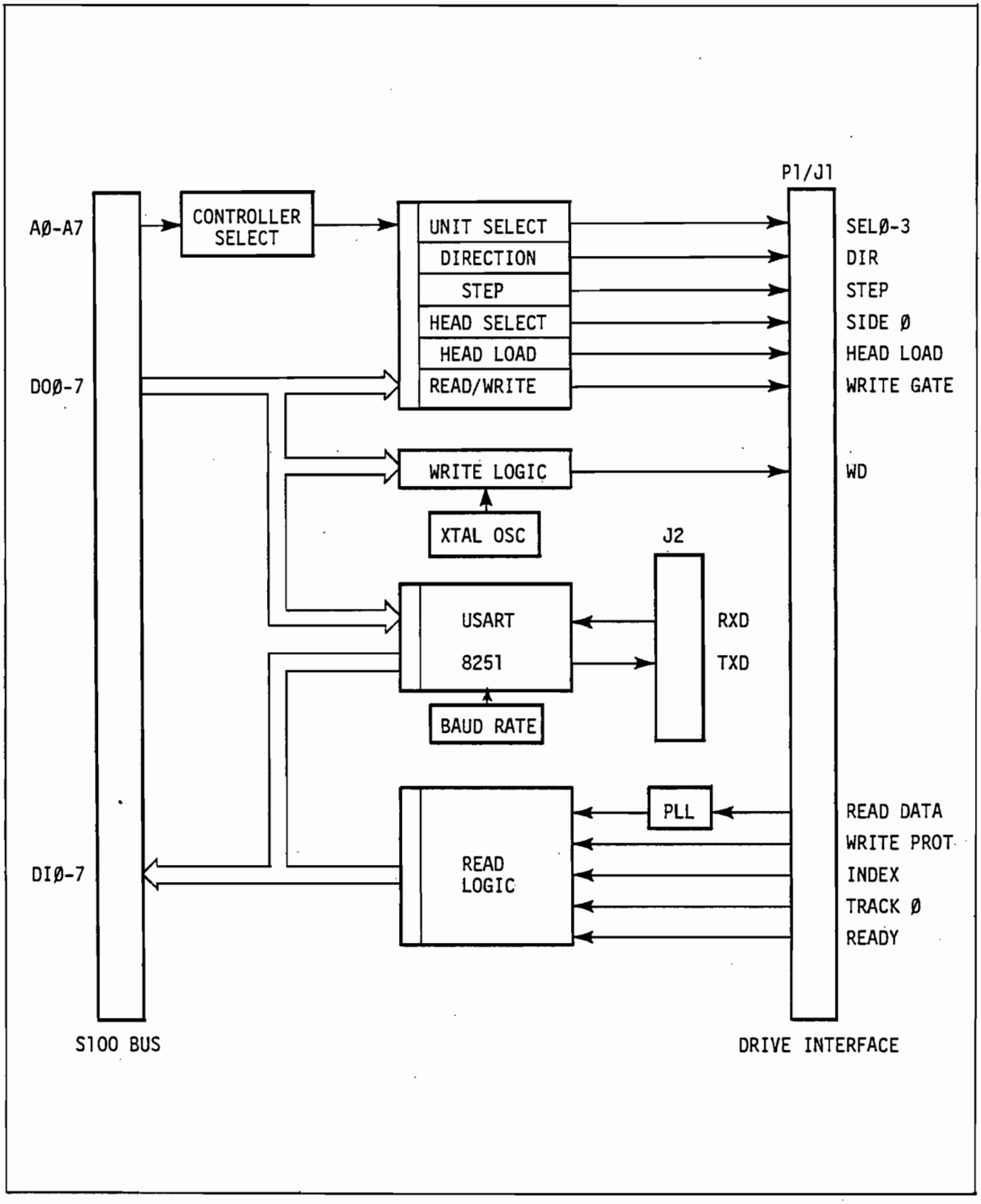


Figure 3-1. 8" Floppy Disk Controller Block Diagram

READ/) during read operations and transfers serial data to the Write Data output during write operations.

Data Register

This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift register.

When executing the Seek command, the Data register holds the address of the desired track position. This register is loaded from the DAL and gated into the DAL under processor control.

Track Register

This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (Towards track 76) and decremented by one when the head is stepped out (toward track 00) if the verify flag is on. The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Sector Register (SR)

This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)

This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a forced interrupt. The command register can be loaded from the DAL, but the contents cannot be placed onto the DAL.

Status Register (STR)

This 8-bit register holds device status information. The meaning of the status bits is a function of the type of command previously executed. This register can be read onto the DAL but cannot be loaded from the DAL.

CRC Logic

This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The CRC includes all information starting with the address mark

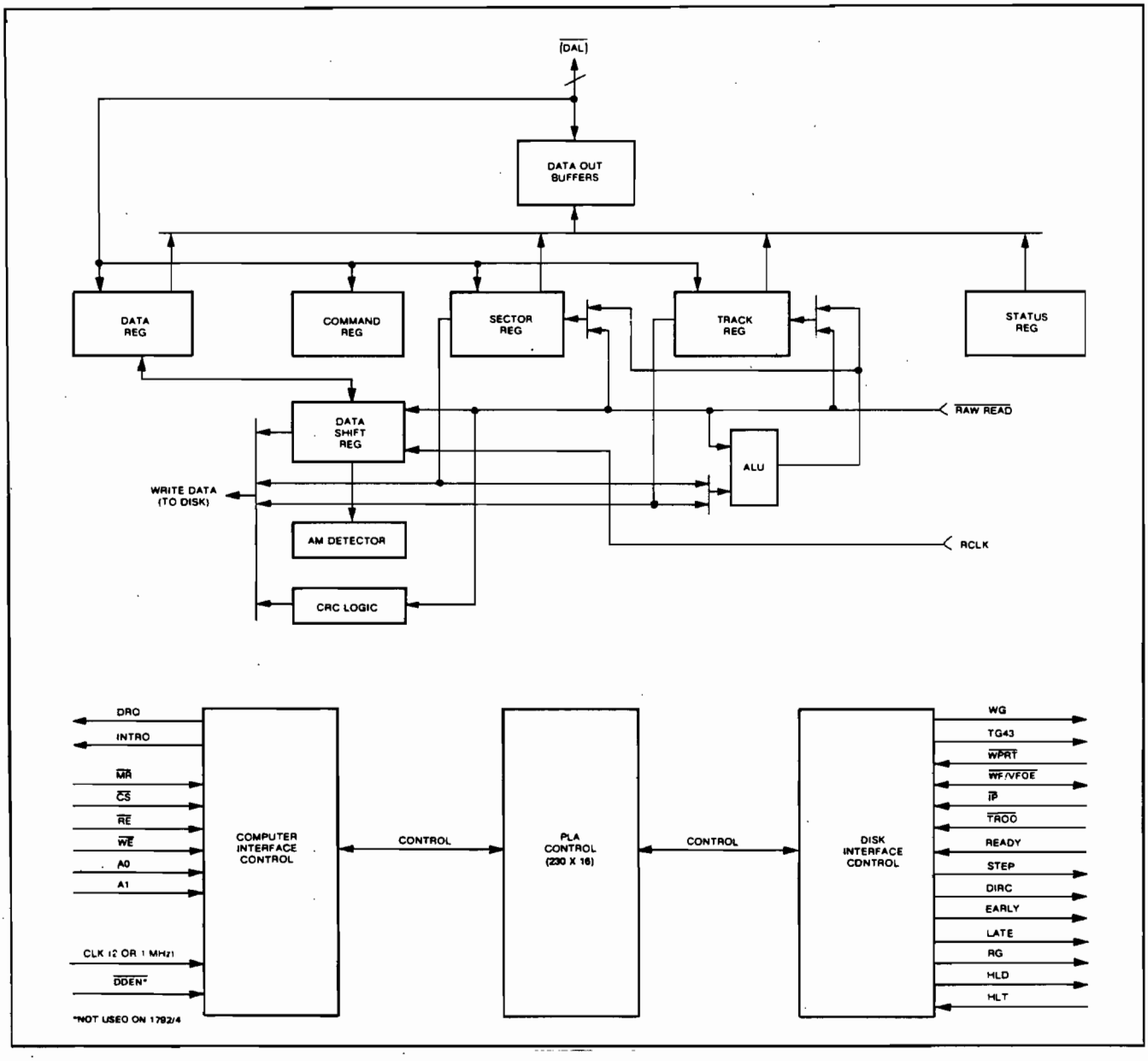


Figure 3-2. Formatter/Controller Block Diagram

and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)

The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control

All computer and Floppy Disk Interface controls are generated through the logic. The internal device timing is generated from an external crystal clock.

The 1793 has two different modes of operation according to the state of DDEN/. When DDEN/ = 0, double density (MFM) is assumed. When DDEN/ = 1, single density (FM) is assumed.

AM Detector

The address mark detector detects ID, data and index marks during read and write operations.

3.9.1 Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines (DAL/) and associated control signals. The DAL/ are used to transfer data, status, and control words out of, or into the 1793. The DAL/ are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE/) are active (low logic state) or act as input receivers when CS/ and Write Enable (WE/) are active.

When transfer data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS/ is made low. The address bits A1 and A0 combined with signals RE/ during a read operation or WE/ during a write operation are interpreted as selecting the following registers:

A1	A0	READ (RE/)	WRITE (WE/)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the 1793 and the processor, the Data Request (DRQ) output is used in Data transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data register. This bit is cleared when the Data Register is read by the processor. If the

Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the lost data bit is set in the Status Register. The Read operation continues until the end of the sector is reached.

On Disk Write operations the data request is activated when the Data Register transfers its contents to the Data Shift register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the lost data bit is set in the Status register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the Status register or by loading the Command register with a new command. In addition, INTRQ is generated if a force interrupt command condition is met.

3.9.2 Floppy Disk Interface

The 1793 has two modes of operation according to the state of DDEN/ (Pin 37). When DDEN/ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK = 1 MHz, these times are doubled.

Head Positioning

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step, an additional 15 ms of head setting time takes place if the verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If TEST/ = 0, there is 0 setting time. There is also a 15 ms head setting time if the E flag is set in any Type II or III command.

The rates (shown in table 1) can be applied to a Step-Direction Motor through the device interface.

Step - A 2 us (MFM) or 4 us (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC) - The direction signal is active high when stepping in and low when stepping out. The direction signal is valid 12 us before the first stepping pulse is generated.

When a Seek, Step, or Restore command is executed, an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond setting time after the head is loaded against the media. The track number from the first encountered ID field is

compared against the contents of the track register. If the track numbers compare and the ID field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The 1793 must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

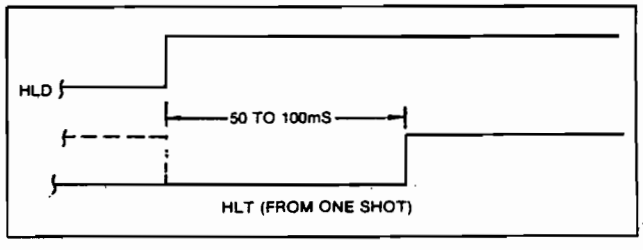
STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	X	X
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	200 µs	400 µs
0 1	6 ms	6 ms	12 ms	12 ms	200 µs	400 µs
1 0	10 ms	10 ms	20 ms	20 ms	200 µs	400 µs
1 1	15 ms	15 ms	30 ms	30 ms	200 µs	400 µs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of a Type I command if the verify flag (V = 1), or upon the receipt of any Type II or III command. Once HLD is active, it remains active until either a Type I command is received with (h = 0 and V = 0); or if the 1793 is in an idle state (non-busy) and 15 index pulses have occured.

Head Load Timing (HLT) is an input to the 1793 which is used for the head engage time. When HLT = 1, the 1793 assumes the head is completely engaged. The head engage time is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the 1793.

HEAD LOAD TIMING



When both HLD and HLT are true, the 1793 will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the 1793 then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

3.9.3 Disk Read Operations

Sector lengths of 128, 256, 512, or 1024 are obtainable in either FM or MFM formats. For FM, DDEN/ should be placed to logical "1." For MFM formats, DDEN/ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this sector length byte in the ID field is 0, then the sector length is 128 bytes. If 01, then 256 bytes. If 02, then 512 bytes. If 03, then 1024 bytes. The number of sectors per track as far as the 1793 is concerned can be from 1 to 255 sectors. The number of tracks as far as the 1793 is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

For read operations, the 1793 requires RAW READ/ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The 1793 must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the 1793 is deriving any useful information from the data stream. Similarly for MFM, RG is made active when four bytes of "00" or "FF" are detected. The 1793 must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the VFOE/ (Pin 33) is provided for phase lock loop synchronization. VFOE/ will go active when:

a) Both HLT and HLD are true.
b) Settling time, if programmed, has expired.
c) The 1793 is inspecting data off the disk.

If WF/VFOE/ is not used, leave open or tie to a 10K resistor to +5.

3.9.4 Disk Write Operation

When writing is to take place on the diskette, the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the data register in response to a data request from the 1793 before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect/ input is a logic low, in which case any write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input,

when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the write gate is activated. On detection of this fault, the 1793 terminates the current command and sets the Write Fault bit (bit 5) in the status word. The Write Fault/ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the 1793 provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM (DDEN/ = 1) and 250 ns pulses in MFM (DDEN/ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written late. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the 1793. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received, the 1793 samples the Ready input. If this input is logic low, the command is not executed and an interrupt is generated. All type I commands are performed regardless of the state of the ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

3.9.5 Command Description

The 1793 will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit (Status bit 0) is off. The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and there Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized below.

3.9.6 Type I Commands

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-out commands. Each of the Type I Commands contains a rate field (r0r1), which determines the stepping motor rate.

The type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the 1793 receives a command that specifically disengages the head. If the 1793 is idle (busy = 0) for 15 revolutions of the disk, the

head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the track register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (status bit 4) is set and the busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the 1793 terminates the operation and sends an interrupt (INTRQ).

The Step, Step-in, and Step-out commands contain an update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

Restore (Seek Track 0)

Upon receipt of this command, the track 00 (TR00/) input is sampled. If TR00/ is active low, indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If TR00/ is not active low, stepping pulses (Pins 15 and 16) at a rate specified by the r1r0 field are issued until the TR00/ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the 1793 terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the restore command is executed when MR/ goes from an active to an inactive state.

Seek

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The 1793 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of thew command. An interrupt is generated at the completion of the command.

Step

Upon receipt of this command, the 1793 issues one stepping pulse to the

disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the U flag is on, the track register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-In

Upon receipt of this command, the 1793 issues one stepping pulse in the direction toward track 76. If the U flag is on, the track register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-Out

Upon receipt of this command, the 1793 issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

3.9.7 Type II Commands

The Type II commands are the Read Sector and Write Sector commands. Prior to loading the Type II command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status bit is set. If the E flag = 1 (this is the normal case), HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.

When an ID field is located on the disk, the 1793 compares the track number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the sector number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into or read from depending upon the command. The 1793 must find an ID field with a track number, sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending on the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 1793 will continue

to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 1793 continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy Status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte, if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is tranferred, that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (bit 5) as shown below.

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

Write Sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and

correct CRC, a DRQ is generated. The 1793 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded into the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the ao field as shown below.

ao	DATA ADDRESS MARK (Bit 0)
1	Deleted Data Mark
0	data Mark

The 1793 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM and MFM. The WG output is then deactivated.

3.9.8 Type III Commands

Read Address

Upon receipt of the Read Address command, the head is loaded and the Busy Status bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte.

Although the CRC characters are transferred to the computer, the 1793 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation, an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the Read Track command, the head is loaded and the busy status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled, it is tranferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track command.

Write Track

Upon receipt of the Write Track command, the head is loaded and the busy status bit is set. Writing starts with the leading edge of the first

encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The data request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data register. If the DR has not been loaded by the time the index pulse is encountered, the operation is terminated making the device not busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

3.9.9 Type IV Command

Force Interrupt

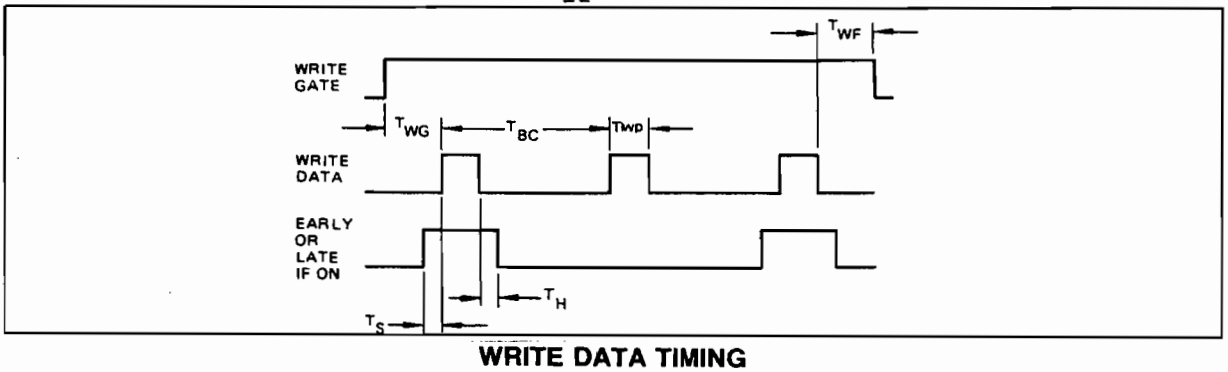
This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition is specified in the Io and I3 field is detected. The interrupt conditions are shown below:

Io = Not Ready-To-Ready Transition
Ii = Ready-To-Not-Ready Transition
I2 = Every Index Pulse
I3 = Immediate Interrupt (requires reset, see note)

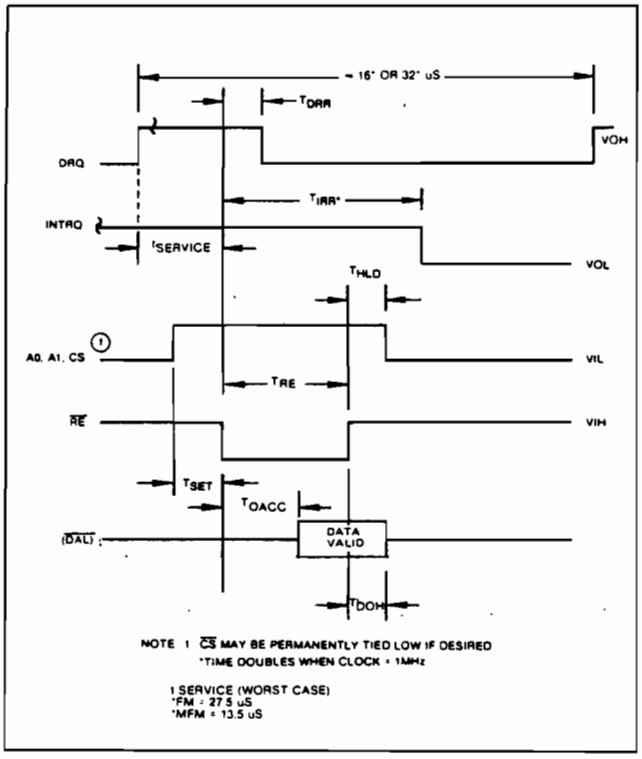
NOTE: If Io - I3 = 0, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.

Status Description

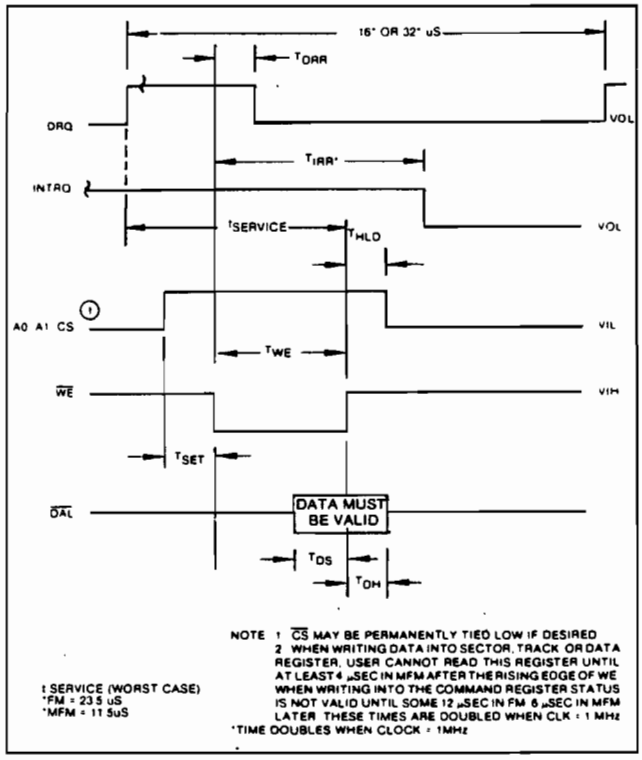
Upon receipt of any command, except the force interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the Status bits are unchanged. If the Force interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, status reflects the Type I commands.



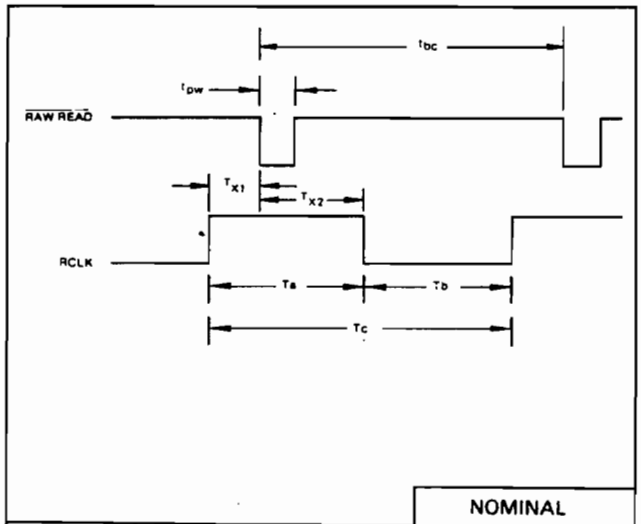
WRITE DATA TIMING



READ ENABLE TIMING

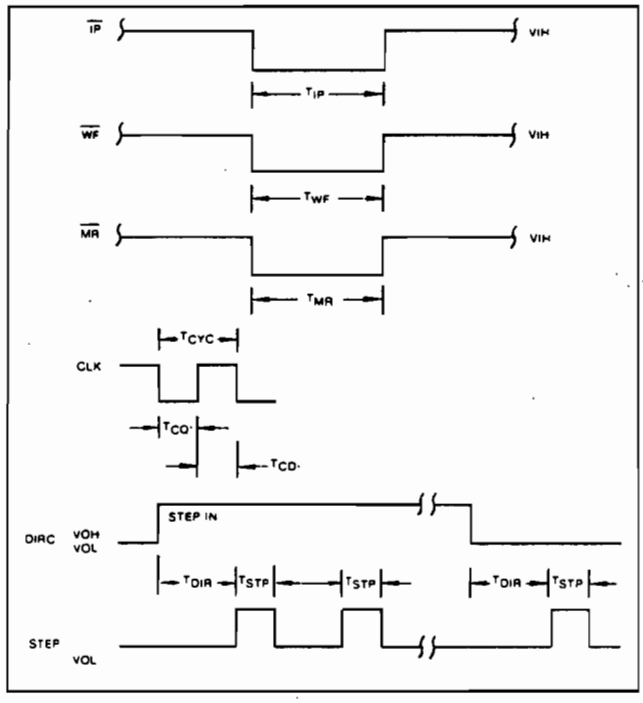


WRITE ENABLE TIMING



				NOMINAL		
DISKETTE	MODE	$\overline{DDEN}$	CLK	T_a	T_b	T_c
8"	MFM	0	2 MHz	1 μS	1 μS	2 μS
8"	FM	1	2 MHz	2 μS	2μS	4 μS
5"	MFM	0	1 MHz	2μS	2μS	4 μS
5"	FM	1	1 MHz	4 μS	4 μS	8 μS

INPUT DATA TIMING



MISCELLANEOUS TIMING

IV. Tests and Adjustments

4.1 Controller Adjustments

Controller adjustments consist of:

a. Center frequency adjust.

b. 1 us single-shot adjust.

c. 0.5 us single-shot adjust.

4.1.1 Test Configuration

a. Insert the controller in an S-100 bus 8080/Z80 based computer using an extender card.

b. Connect controller to any Data Trak 8 storage module.

4.1.2 Center Frequency Adjust Test Procedure

a. Ensure that the drive is not on.

b. Connect oscilloscope to oscillator at A15-7. Set oscilloscope time base to 200 ns/cm.

c. Measure frequency of oscillator.

4.1.3 1 us Single-Shot Adjust Test Procedure

a. Insert a diskette in drive.

b. Position the head to track 0 and write a full track of 'ones' data (16 sectors).

c. Perform a continuous read operation on track zero.

d. Alternately select program X14 to achieve steps b and c.

e. Connect oscilloscope to A14-5. Set time base of oscilloscope to 200 ns/cm and observe one-shot output.

4.1.4 0.5 us Single-Shot Adjust Test Procedure

a. Proceed with steps a thru d, paragraph 2.1.3.

b. Connect oscilloscope to A14-3. Set time base of oscilloscope tp 200 ns/cm and observe one-shot output.

4.1.5 Acceptable Limits

a. Center Frequency: 970 KHz minimum - 1033 KHz maximum.

b. 1 us single-shot: 1.94 us minimum - 2.06 us maximum.

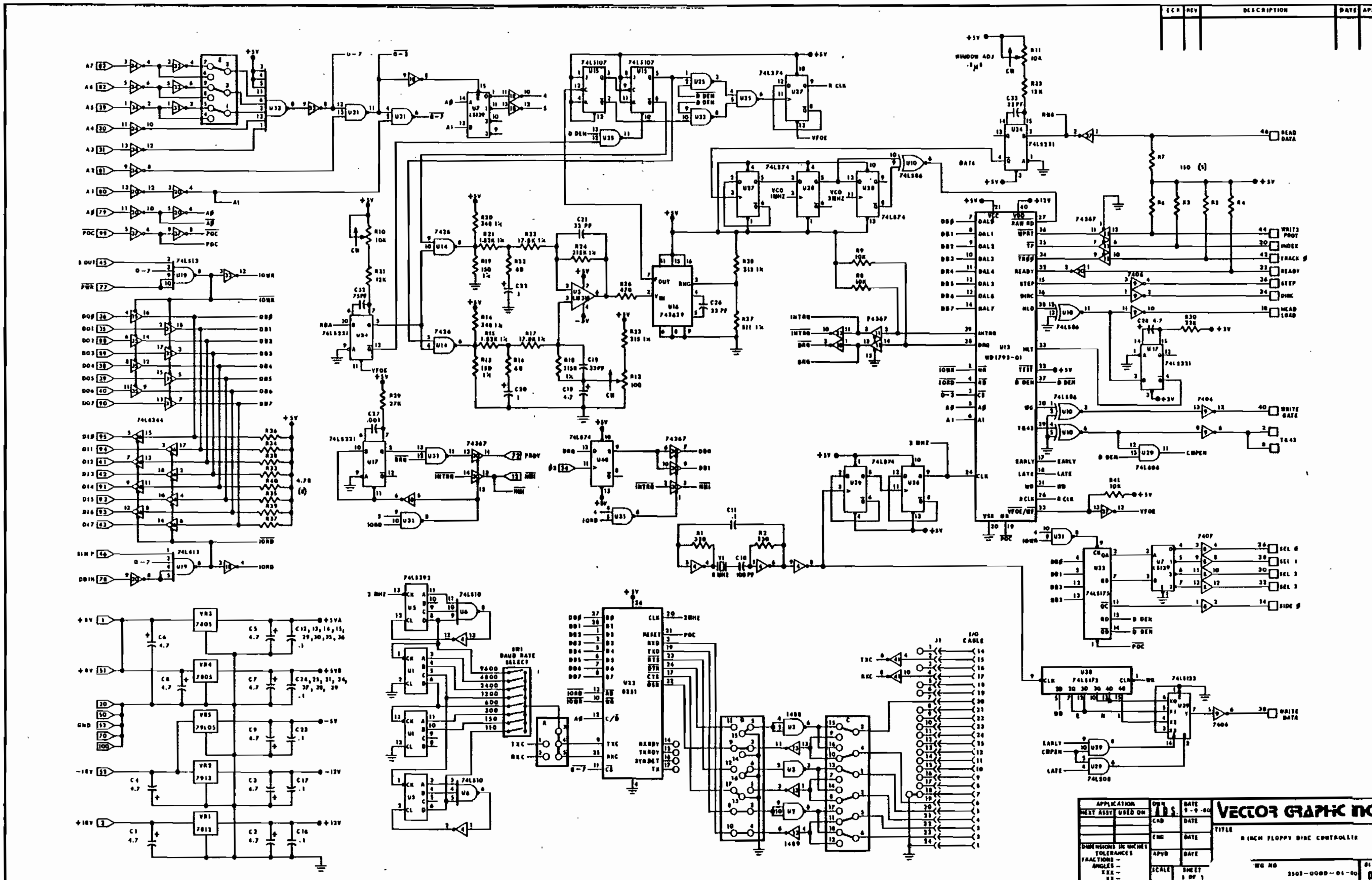
c. 0.5 us single-shot: 0.97 us minimum - 1.03 us maximum.

4.1.6 Adjustment Procedure

a. Center frequency: Adjust R40 until output frequency is 0.5 MHz.

b. 1 us single-shot: Adjust R27 for a period of 1 us.

c. 0.5 us single-shot: Adjust R46 for a period of 0.5 us.



VECTOR GRAPHIC INC.
TITLE
8 INCH FLOPPY DISC CONTROLLER
DWG NO
3503-0000-01-00
SIZE
D
SHEET
1 OF 1
APPLICATION
NEXT ASSY
USED ON
DIMENSIONS IN INCHES
TOLERANCES
FRACTIONS
ANGLES
DATE
CHD
ENG
APVD
SCALE
ECR
REV
DESCRIPTION
DATE
APPD