TARBELL CPU/IO BOARD MODEL 3033

OWNER'S MANUAL

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Tarbell Z-80 CPU Introduction April 8, 1981

The Tarbell Z-80 CPU board is designed to use the full power of the Z-80 CPU chip along with 2 serial ports, a timer chip, 8080 vector interrupt or Z-80 mode 2 interrupt, and extended memory management of 1 Megabyte with the capability of relocation on 4 Kbyte boundrys. The Tarbell Z-80 CPU board is designed around the IEEE S-100 standard and is directly compatible with all products sold by Tarbell Electronics.

The Tarbell Z-80 CPU board will run at either 2 MHz or 4 MHz by means of a jumper selection on the board.

The on-board timer, which is an 8253 timer chip, will generate timing intervals from 1 micro-sec. to 327 milli-sec. using 1 of the 3 timers available in the 8253. Provisions are made on the CPU board to chain the additional 2 timers together for increased time intervals. The 2 additional timers may also be used independantly of the others.

The Tarbell Z-80 CPU has provisions for accepting 8080 vector restarts. The level of interrupt is also maskable with one exception in that neither RST 0 or RST 7 are maskable because of their use in CPM (r). The other 6 restarts are maskable by way of a register on an I/O port on the CPU board. As an option jumper, provisions have been made to allow the Mode 2 interrupt of the Z-80 to function.

The CPU board uses 2 8251 usarts for serial I/O operation. Each channel's baud rate is set by an on-board switch which controls an SMC-5016 baud rate chip. Baud rates from 50 to 19,200 are switch selectable for each channel. Each serial channel is RS-232 compatible with hand-shaking provided for DTR,RTS, DSR, and CTS lines.

One unique feature of the Tarbell Z-80 CPU is it's Memory Management circuit. By using a ram mapping techinque, we can make the Z-80 appear to address 1 Megabyte address range, even though the Z-80 will only address 64 Kbytes directly. Besides the main advantage of being able to address 1 Megabyte of memory, the ram mapping technique also allows the programmer the ability to relocate software on 4 Kbyte boundries for dynamic memory allocation schemes.

Port assignments for the on-board I/O, Timer, Vector Interrupt mask port, and Memory Management are determined by jumpers E4, E5, and E6. When jumper E4 to E5 is connected, the base address for the I/O, Timer, and Vector Interrupt mask port starts at base 00 hex and the Memory Management ports start at 20 hex.

When jumper E4 to E6 is connected, the base address for the I/O, Timer, and Vector Interrupt mask port starts at 10 hex and the Memory Management ports start at 30 hex.

A breakdown of the ports and use will be described below.

Base address = 00 hex (jumper E4 to E5)

Port	use	operation
00 hex	serial port A	input/output data port
01 hex	serial port A	input status port/output init.
02 hex	serial port B	input/output data port
03 hex	serial port B	input status port/output init.
04 hex	counter 0	input/output
05 hex	counter 1	input/output
06 hex	counter 2	input/output
07 hex	counter command port	output only
08 hex	interrupt latch clear	input only
09 hex	interrupt mask port	output only
0A hex	enable memory mang.	output only
0B hex	disable memory mang.	input only
0C hex	not used	
0D hex	not used	
0E hex	not used	
0F hex	not used	

The Memory Management ports will be addressed starting at 20 H OR 30 H hex.

Port	use	operation
20 to 2F hex	init. memory mangement	output only, ram mapping info.

TO 3FH

The initialization bytes for the memory management are as follows.

Port	Byte
20 hex	FF hex
21 hex	FE hex
22 hex	FD hex
23 hex	FC hex
24 hex	FB hex
25 hex	FA hex
26 hex	F9 hex
27 hex	F8 hex
28 hex	F7 hex

29 hex	F6 hex
2A hex	F5 hex
2B hex	F4 hex
2C hex	F3 hex
2D hex	F2 hex
2E hex	F1 hex
2F hex	F0 hex

Because the ram on the CPU card can come up in any random bit pattern when power is first applied, the above initialization bytes must be sent out to set the ram into a known state before turning on the memory management for use. The above pattern sets the memory management for normal access to 64 Kbytes of system memory, and disables memory above 64 Kbytes by setting A16,A17,A18, and A19 to all zeros.

When the board is first powered up, the memory management is not enabled and the full 64 kbyte address space may accessed as if the memory management did not exist at all. In order to use the memory management, it must be initialized first, then turned on.

The Tarbell CPU may run at either 2 MHz or 4 MHz .

CPU Speed select

For 2 MHz operation - connect center to E2 *
For 4 MHz operation - connect center to E1

I/O Base Address Select

The base address of the onboard I/O ports may be set for either a base of 00 hex or a base of 10 hex. This allows you to move the CPU I/O ports to avoid any conflict which may exist with other boards in your system which use either of these base addresses.

For an I/O base of 00 hex - connect E4 to E5 *
For an I/O base of 10 hex - connect E4 to E6

Vector Interrupt Options

Two methods of vector interrupts may be used on this CPU board, but only one may be active at a time. One method is the normal 8080 interrupt vector which activates one of the restart vector lines on the S-100 bus. The other method uses the interrupt Mode 2 of the Z-80 and activates only the S-100 interrupt line (pin 73).

8080 interrupt mode - E16 open *
Z-80 interrupt mode 2 - E16 closed

NMI (Non-maskable Interrupt) Option

The non-maskable interrupt option has 3 possible configurations you may consider to use. As a note of caution, because the non-maskable interrupt of the Z-80 is locked to location 66 hex, the possibility of use while running CP/M does not look feasible because this location happens to be right in the middle of the file control block used by CP/M for file access. If you plan to use this CPU card in a stand-alone type system, then the whole situation is different. Typical uses for non-maskable interrupts are to monitor for power failures, errors due to parity bits in error, or monitoring hardware events which must have the highest possible priority in a system.

The three options are as follows:

Jumper E18 - NMI\ (direct input to Z-80 NMI pin.)
Jumper E19 - PWRFAIL\ (system type power fail indicator.)
Jumper E20 - ERROR\ (any status signal indication an error occured.)

Because these lines are suppose to be driven with open collector drivers, any or all of these jumpers may be tied together.

I/O Interrupts option

Each serial channel has provisions for generating an interrupt if needed. The outputs are all open collector, so they may be connected wired-or if you plan on using 1 interrupt line.

Interrupt		Connection
Channel A		
Recieve Ready	(RxRDY)	I5
Transmitter Ready	(TxRDY)	I4
Transmitter Empty	(TxE)	I2
Channel B		
Recieve Ready	(RxRDY)	I6
Transmitter Ready	(TxRDY)	I1
Transmitter Empty	(TxE)	I3

Timer options

The onboard timer has only 1 of the 3 internal timers committed. This timer is committed for use in generating an interrupt. This timer chip is driven by an external clock input frequency of 2 MHz from the CPU internal clock. The timer committed for this function is timer channel 2. The output of the timer sets a latch which drives the input of an 7406 open collector inverter. The output of the inverter may be connected to any of the 8 vector interrupt input lines (VI0 to VI7). The latch is cleared by executing an input from port BASE+8 hex in your interrupt routine, where BASE is the base address you have chosen to use for your I/O port base.

The other 2 timers are available for general use with all the inputs available to each section of each timer. These 2 timers may be chained together for long time intervals, or may be used independently. For further information about the use of these timers, please refer to the end of this manual to the data sheets on the 8253 timer chip.

Below is a table of the jumpers for the unused timers.

E24 - counter 0 GATE input (pull up for enable if jumpered)
E25 - counter 1 GATE input (pull up for enable if jumpered)
E28 - counter 0 OUTPUT
E29 - counter 1 OUTPUT
E26 - counter 0 CLOCK input
E27 - counter 1 CLOCK input

Memory Management Option

The memory management is invisible when the CPU is first brought up in your system. You have the full 64K address space ot the Z-80 cpu and will operate as a normal cpu card. This happens because the system reset clears the memory management to an off state.

To use the memory management on the CPU board, you must first initilize the on board memory chips as described in section 4 of this manual. After you have set the memory management chips up, you can enable it by doing an output instruction to port BASE+0A hex.

You may turn off the memory management at any time by doing an input instruction from BASE+0B hex. This will turn off the memory management circuit and you will have a normal 64K address space.

Mwrite

If your computer system does not have provisions for the generation of the Mwrite signal, you will find it generated on our CPU board. To enable this signal onto pin 68 of the S-100 bus, jumper E7 to E8. This signal is required by most memory boards in use today.

Used non-defined pins of S-100 bus

Pin 21

To effectivly use the Z-80 interrupt Mode 2 with it's support I/O chips, the signal IORQ\ is needed. This signal can be made available on pin 21 by jumpering E9 to E10.

The signal MREQ\ is also available by jumpering E11 to E10. This signal may be used by some dynamic memory boards in the future.

Pin 27

This line is being used for providing PWAIT for front panels. To use this feature jumper E12 to E13.

Pins 71 and 69

As part of the interrupt Mode 2 usage, some provision must be made for the daisy-chain of the Interrupt lines from each Z-80 support chip to the next. We would like to promote a standard which uses pin 71 as the IEI (interrupt enable input) line, and pin 69 as the IEO (interrupt enable output) line. This convention will be used for any support products which use any of the Z-80 I/O chips by Tarbell Electronics and Delta Products. We hope this will encourage other designers in the same direction.

Pin 66

Some dynamic memory boards have provisions for refreshing by using the Z-80 refresh signal. This signal may be made availble to pin 66 by jumpering E14 to E15.

Wait States

Three options exist for wait states if needed.

1. I/O wait states
2. M1 wait states
3. Memory wait states.

The on board wait state generator only provideds 1 wait state and you may select any or all if needed. To select an wait state for I/O operations, jumper E23. To select an wait state for M1 cycles, jumper E21. To select an wait state for all memory cycles, jumper E22.

The on-board serial ports are a pair of 8251's with full RS-232 handshaking. Each serial port has it's own baud rate generator which is controlled by an SMC-5016 baud rate generator. The baud rate is set in hardware by dip switch S-xx. The top four switch positions control Channel A baud rate, and the bottom four switch positions control Channel B baud rate. The layout of the switches are as follows.

```
        S-xx

   A    [--] ---
   B    [--]   Chan
   C    [--]    A
   D    [--] ---
   A    [--] ---
   B    [--]   Chan
   C    [--]    B
   D    [--] ---
```

The following table shows the switch settings for desired baud rate.

Baud Rate	A	B	C	D
50	on	on	on	on
75	off	on	on	on
110	on	off	on	on
134.5	off	off	on	on
150	on	on	off	on
300	off	on	off	on
600	on	off	off	on
1200	off	off	off	on
1800	on	on	on	off
2000	off	on	on	off
2400	on	off	on	off
3600	off	off	on	off
4800	on	on	off	off
7200	off	on	off	off
9600	on	off	off	off
19200	off	off	off	off

Handshaking for the two serial ports is provided by the RS-232 line drivers and line receivers which are 1488's and 1489's by way of connector J2 at the top of the board. A break down of this connector is as follows:

J2 pin number	channel	function	in/out
1	A	ground	
2	A	ground	
3	A	transmit data	output

4	A	data terminal ready	output
5	A	request to send	output
6	A	receive data	input
7	A	data set ready	input
8	A	clear to send	input
9		+5 volts	
10		+12 volts	
11		-12 volts	
12		ground	
13	B	transmit data	output
14	B	data terminal ready	output
15	B	request to send	output
16	B	receive data	input
17	B	data set ready	input
18	B	clear to send	input
19	B	ground	
20	B	ground	

The I/O cable coming from the 20 pin connector on the CPU card to the pair of DB-25 connectors is defined as follows:

	RS-232 pin connector		20 pin connector
--	(2)	Xmit Data (from cpu)	3
	(3)	Recv Data (to cpu)	6
	(4)	Rts	5
A port	(5)	Cts	8
	(6)	Dsr (handshake line)	7
	(7)	Gnd	1,2
--	(20)	Dtr	4
		+5	9
pull up's		+12	10
		-12	11
--	(2)	Xmit Data (from cpu)	13
	(3)	Recv Data (to cpu)	16
	(4)	Rts	15
B port	(5)	Cts	18
	(6)	Dsr (handshake line)	17
	(7)	Gnd	19,20
--	(20)	Dtr	14

Note: Software from Tarbell Electronics looks at DSR (pin 6 of RS-232 line), for handshaking with printers. This line is active low when the printer buffer full flag is active. This means that the cpu should stop sending characters until DSR goes high again. Some printers use Dtr (pin 20 of RS-232 line) as the handshake line back to the cpu. You should jumper pin 20 on the back side of the RS-232 connector board to pin 6 of the 20 pin connector. A hole has been provided for this connection. Some printers use the Alternate clear to send line on the RS-232 lines. This is usually pin pin 19 of the RS-232. This line should be connected to DSR (pin 6 of the 20 pin

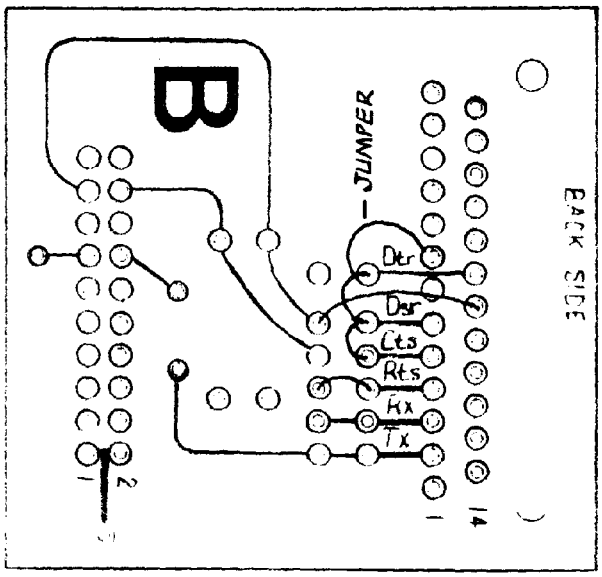
connector for proper handshaking). Some printers use clear to send for handshaking. If this is the case, you should jumper the clear to send line (pin 5 of the RS-232 line) to the DSR line (pin 6 of the 20 pin connecter) for proper handshaking.

If you are going to use a CRT on one port and a printer on the other, we would like to recommend that you use Chan A for the CRT port and Chan B for the printer port. This is the normal configuration that we here at Tarbell Electronics will be using in our software. The CRT port will use transmit data (J2 pin 3), receive data (J2 pin 6), and ground. The printer port will use transmit data (J2 pin 13),and some sort of buffer full handshaking, probably data set ready (J2 pin 17), and a ground. You should consult your printer and terminal manuals for any problems you may have.

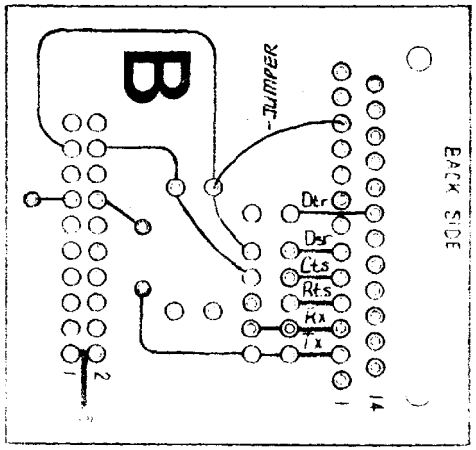
As a service to our customers, we have provided some of the common printer configurations that we have checked out here. All of these configurations use the channel B port for the printer. As we become use other printers on the market, we will provide that information as well.

Page 4 starts the printer configuration section.

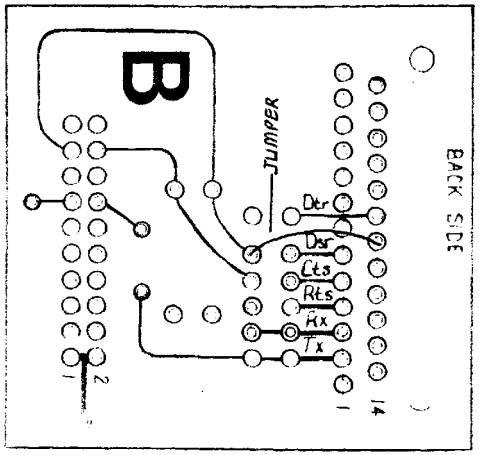
NEC SPINWRITER



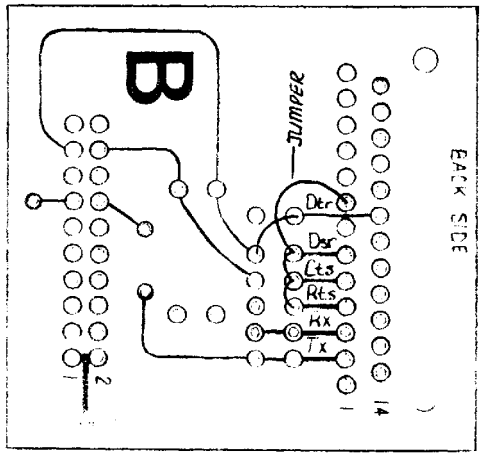
EPSON MX-80



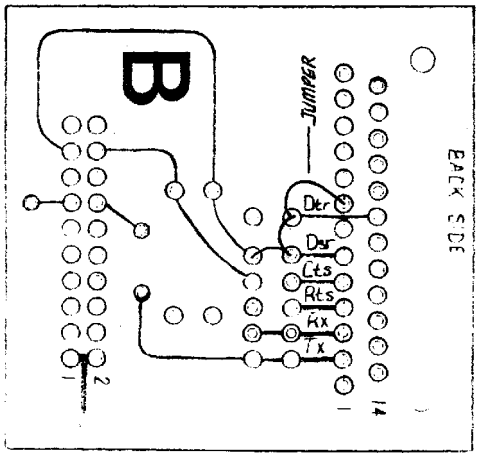
ANADEX 9501



DIABLO 1640



TI - 810



The on-board memory which is used for the Memory Management must be initialized before it is used. In order to use the CPU board in a normal 64 Kbyte system, the memory management would have to be set using the following subroutine.

```
COUNT   EQU     16              ;16 values to move.
MEMENB  EQU     0AH             ;enable port.
MEMPORT EQU     20H             ;either 20 Hex or 30 Hex for memory
                                ;management port base.
;
INIT:   LXI     D,TABLE         ;point to memory discriptor table.
INIT1:  LXI     B,COUNT SHL 8 OR MEMPORT
ILOOP:  LDAX    D               ;get a byte from table.
        CMA                     ;compliment it for on-board memory.
        OUTP    A               ;output it to memory.
        INR     C               ;bump port number to next.
        INX     D               ;point to next byte in table.
        DJNZ    ILOOP           ;and loop 16 times till done.
        OUT     MEMENB          ;turn on memory management.
        RET                     ;return to caller.
;
TABLE:  DB      00H,01H,02H,03H,04H,05H,06H,07H,08H
        DB      09H,0AH,0BH,0CH,0DH,0EH,0FH
```

Now the situation arises where you may have multi-users on your system. You first will have to establish what users will be in what groups of memory at any user time slice. For example, you have 4 64 Kbyte memory boards. Your operating system will need 16 Kbytes of common memory for file operations. This will leave you with 48 Kbytes of user memory. This means that you will have 3 16 Kbyte blocks left over, 1 16 Kbyte block from each 64 Kbyte group. With these 3 16 Kbyte blocks, you would be able to run 5 users on your system, with each user sharing the one common area of the operating system. The following subroutine could be used to manage the memory useage.

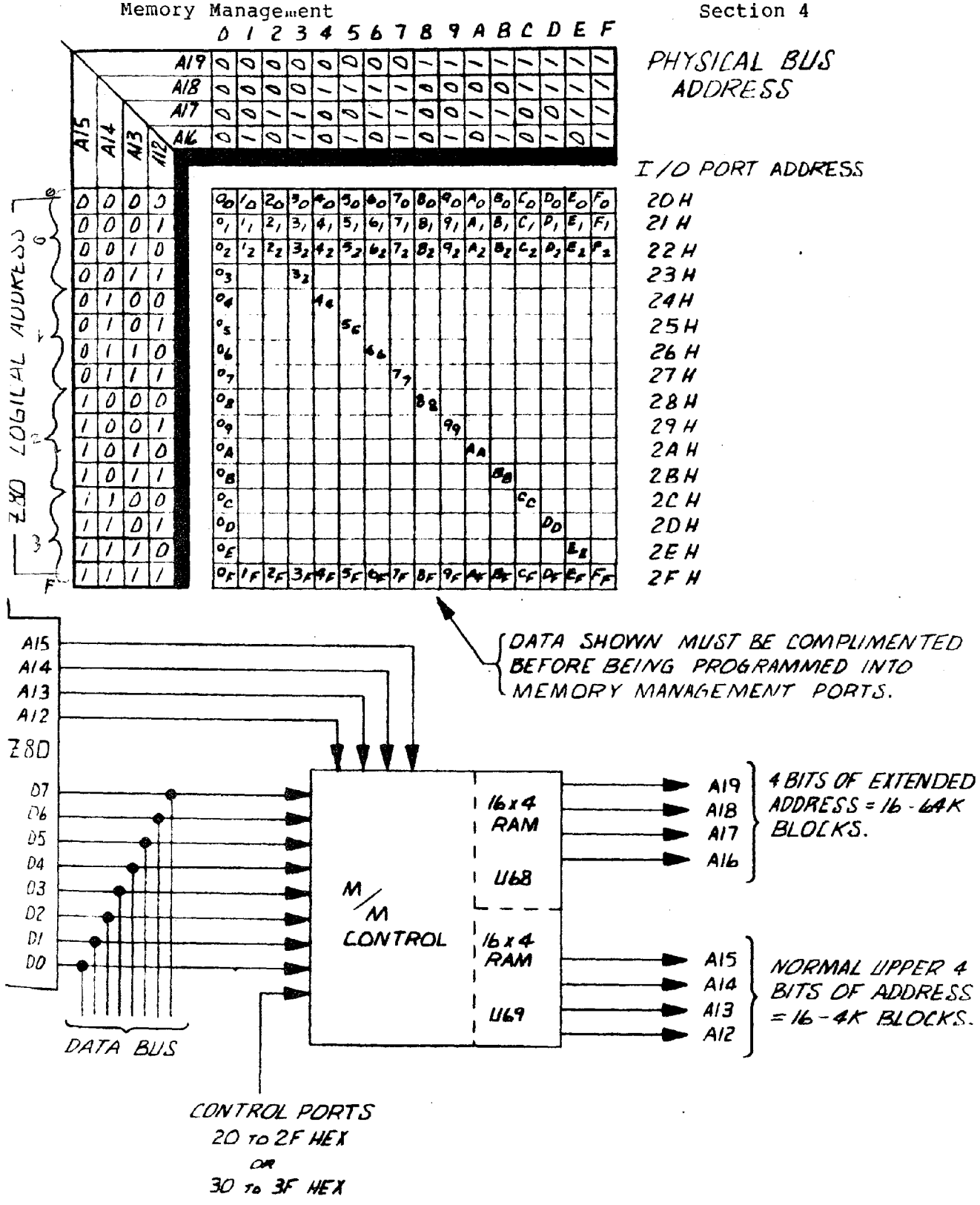
```
BANKSSWITCH:
;
;Entry  Reg A = user number (0 to 4)
;Exit   User bank selected
;
        ADD     A               ;double for computed index.
        LXI     H,TABLE         ;point to start of table pointers.
        MOV     C,A             ;set up B,C for offset.
        MVI     B,0             ;zero REG B.
        DAD     B               ;H,L = User table value.
        LXI     B,COUNT SHL 8 OR MEMPORT        ;count, port.
BANKL:  MOV     A,M             ;get memory init byte.
        CMA                     ;invert for on-board memory chips.
        OUTP    A               ;program the memory management.
        INX     H               ;bump pointer.
        INR     C               ;bump memory management port.
        DJNZ    BANKL           ;loop till done.
        RET                     ;return to caller.
```

The on-board memory which is used for the Memory Management must be initialized before it is used. In order to use the CPU board in a normal 64 Kbyte system, the memory management would have to be set using the following subroutine.

```
COUNT   EQU     16              ;16 values to move.
MEMENB  EQU     0AH             ;enable port.
MEMPORT EQU     20H             ;either 20 Hex or 30 Hex for memory
                                ;management port base.
;
INIT:   LXI     D,TABLE         ;point to memory discriptor table.
INIT1:  LXI     B,COUNT SHL 8 OR MEMPORT
ILOOP:  LDAX    D               ;get a byte from table.
        CMA                     ;compliment it for on-board memory.
        OUTP    A               ;output it to memory.
        INR     C               ;bump port number to next.
        INX     D               ;point to next byte in table.
        DJNZ    ILOOP           ;and loop 16 times till done.
        OUT     MEMENB          ;turn on memory management.
        RET                     ;return to caller.
;
TABLE:  DB      00H,01H,02H,03H,04H,05H,06H,07H,08H
        DB      09H,0AH,0BH,0CH,0DH,0EH,0FH
```

Now the situation arises where you may have multi-users on your system. You first will have to establish what users will be in what groups of memory at any user time slice. For example, you have 4 64 Kbyte memory boards. Your operating system will need 16 Kbytes of common memory for file operations. This will leave you with 48 Kbytes of user memory. This means that you will have 3 16 Kbyte blocks left over, 1 16 Kbyte block from each 64 Kbyte group. With these 3 16 Kbyte blocks, you would be able to run 5 users on your system, with each user sharing the one common area of the operating system. The following subroutine could be used to manage the memory useage.

```
BANKSWITCH:
;
;Entry  Reg A = user number (0 to 4)
;Exit   User bank selected
;
        ADD     A               ;double for computed index.
        LXI     H,TABLE         ;point to start of table pointers.
        MOV     C,A             ;set up B,C for offset.
        MVI     B,0             ;zero REG B.
        DAD     B               ;H,L = User table value.
        LXI     B,COUNT SHL 8 OR MEMPORT        ;count, port.
BANKL:  MOV     A,M             ;get memory init byte.
        CMA                     ;invert for on-board memory chips.
        OUTP    A               ;program the memory management.
        INX     H               ;bump pointer.
        INR     C               ;bump memory management port.
        DJNZ    BANKL           ;loop till done.
        RET                     ;return to caller.
```


PHYSICAL BUS ADDRESS
I/O PORT ADDRESS
Z80 LOGICAL ADDRESS
20 H
21 H
22 H
23 H
24 H
25 H
26 H
27 H
28 H
29 H
2A H
2B H
2C H
2D H
2E H
2F H
DATA SHOWN MUST BE COMPLIMENTED BEFORE BEING PROGRAMMED INTO MEMORY MANAGEMENT PORTS.
A15
A14
A13
A12
Z80
D7
D6
D5
D4
D3
D2
D1
D0
DATA BUS
M/M CONTROL
16x4 RAM
U68
16x4 RAM
U69
A19
A18
A17
A16
4 BITS OF EXTENDED ADDRESS = 16 - 64K BLOCKS.
A15
A14
A13
A12
NORMAL UPPER 4 BITS OF ADDRESS = 16 - 4K BLOCKS.
CONTROL PORTS
20 TO 2F HEX
OR
30 TO 3F HEX

CPU/IO BOARD
REV E
BAUD
4 MHZ
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Qty.	Descriptor	Designator
Resistors		
2	62 ohm 1 watt	R1,R2
3	330 ohm 1/4 watt	R11,R14,R15
15	1 K ohm 1/4 watt	R3,R4,R7,R10,R12,R13,R16,R17 R18,R19,R20,R21,R22,R23,R24
4	4.7 K ohm 1/4 watt	R5,R6,R8,R9
2	NW-15-1K Resistor pack	U40,U51
1	NW-15-4.7K Resistor pack	U48
Capacitors		
20	.1 Mfd >10 volts	C3,C4,C5,C7,C8,C9,C10,C11,C12 C15,C16,C17,C18,C19,C20,C21,C22 C23,C24,C25
4	10 Mfd 16 volt	C1,C2,C13,C14
1	22 Mfd 10 volt	C6
Misc.		
1	DIP-SW8 8 position dip switch	U35
1	HDR-20 20 pin header	J2
57	PIN Jumper pins	E jumpers
10	BLOCK Jumper blocks	E jumpers
1	LM-323 Regulator	VR1
1	TO-3 Heatsink	for VR1
1	TO-3 Heatsink top	for VR1
2	1N4742 Zener diode (12 volts)	CR1,CR2
1	XTL-16 16.00 Mhz crystal	Y1
1	XTL-5.0688 5.0688 Mhz crystal	Y2
Hardware		
2	6-32 x 3/8 screw	
2	#6 washer	
2	#6 nuts	
2	2-56 x 1/2 screw	
2	#2 washer	
2	#2 nuts	
1	40 pin socket	
2	28 pin socket	
1	24 pin socket	
10	20 pin socket	
1	18 pin socket	
11	16 pin socket	
24	14 pin socket	

IC's

2	7400/74LS00	Quad 2-input nand gate	U29,U33
1	7402/74LS02	QUAD 2-Input nor gate	U31
3	7404/74LS04	Hex inverter	U2,U8,U12
1	74S04	High speed Hex inverter	U36
2	7406	O/C Hex inverter	U6,U10
2	7408/74LS08	Quad 2-input and gate	U13,U34
1	7410/74LS10	Triple 3-input nand gate	U19
1	74LS14	Hex schmitt triggger	U9
4	7432/74LS32	Quad 2-input or gate	U5,U25,U30,U39
3	7474/74LS74	D toggle flip-flop	U14,U20,U28
1	82S123/6331	Prom (prom # 109)	U18
1	74138/74LS138	3 to 8 line decoder	U4
1	74148/74LS148	8 line to 3 line encoder	U26
1	74161/74LS161	Binary counter	U21
1	74174/74LS174	6 bit latch	U27
2	74S189	16 x 4 memory chip	U41,U42
9	74LS244	Octal tri-state buffer	U17,U43,U44,U4 U46,U47,U49,U5 U52
2	74LS260	5 input nor gate	U1,U3
1	8T98/74368	Hex inv. tri-state buffer	U15
2	MC1488/SN75188	RS-232 interface	U22,U24
2	MC1489/SN75189	RS-232 interface	U11,U23
1	8304/8286	Octal bi-directional driver	U32
2	8251AC	Programmable USART	U37,U38
1	8253C-5	Programmable TIMER	U54
1	SMC5016/BR1941-1	Baud rate generator	U53
1	Z80A	Central Processor	U16

Tarbell Z-80 CPU Board Full 6 Month Warranty

1. Any faulty component part purchased from Tarbell Electronics, which is returned within 6 months after the date of purchase will be replaced at no charge. Components returned under this part of the warranty should be with a letter explaining what is wrong with the part.

2. Any factory-assembled Z-80 CPU interface, which does not work correctly, and is returned within 6 months after the date of purchase, will be restored to proper operating condition or replaced without charge.

3. Any Z-80 CPU interface kit, which in the opinion of the manufacturer has been assembled with reasonable care, and is returned for repair within 6 months after the date of purchase, will be repaired for a charge commensurate with the work required, (parts will be free) but in no case will exceed $100 without notification of the owner.

4. Any Z-80 CPU interface not covered by the above condition will be subject to a charge commensurate with the work and parts required, but in no case wil exceed $100 without notification of the owner.

5. Parts can be returned directly to the address below for replacement. Complete Z-80 CPU interfaces should be returned to the place of purchase. If this is not possible, or if it is very inconvenient, it may be returned to the address below, with proof of purchase.

6. Tarbell Electronics assumes no responsibility for consequential damages to other connected equipment, or for time lost, or programs or data lost, because of CPU malfunction or incorrect documentation.

7. If you are disatisfied with the operation of a factory-assembled Tarbell Z-80 CPU Interface Board for any reason, your money will be cheerfully refunded, provided the unit is returned within the six month warranty period.

8. Tarbell Electronics does not warrant that the CPU interface will work with all "S-100" computer systems. Call the factory or ask your local dealer about any possible conflicts in your system.

9. This warranty does not cover parts, or interfaces built from parts, which are not traceable to Tarbell Electronics.

10. A CPU which is assembled from a kit by a Tarbell dealer has only the parts covered by this warranty, not the labor. All CPU's which were sold as kits, will have a "K" marked on the solder side. The dealer may provide his own warranty in this case.

Defective parts or CPU's covered under this warranty should be sent WITH PROOF OF PURCHASE (like a receipt) to:

Tarbell Electronics
950 Dovlen Place, Suite B
Carson, California 90746

IEEE Specification, IEEE Task 696.1/D2

The following is a list of the IEEE pin functions, signals, type of signal, active level, and a description of the signal.

The following conventions will be used:

1. \ = inverted signal or the NOT function.
2. M = master.
3. B = bus.
4. S = slave.
5. O.C. = open collector.
6. H = high or logic level 1
7. L = low or logic level 0

Pin	Signal	Type	Active Level		Description
1	+8 volts	B			Instantaneous min greater than 7 volts, instantaneous max less than 25 volts, average max less than 11 volts.
2	+16 volts	B			Instantaneous min greater than 14.5 volts, instantaneous max less than 35 volts, average max less than 21.5 volts.
3	XRDY	S	H		One of two ready inputs to the current bus master. The bus is ready when both inputs are true (H). see pin 72.
4	VI0\	S	L	O.C.	Vectored interrupt line 0.
5	VI1\	S	L	O.C.	Vectored interrupt line 1.
6	VI2\	S	L	O.C.	Vectored interrupt line 2.
7	VI3\	S	L	O.C.	Vectored interrupt line 3.
8	VI4\	S	L	O.C.	Vectored interrupt line 4.
9	VI5\	S	L	O.C.	Vectored interrupt line 5.
10	VI6\	S	L	O.C.	Vectored interrupt line 6.
11	VI7\	S	L	O.C.	Vectored interrupt line 7.
12	NMI\	S	L	O.C.	Non-maskable interrupt line.
13	PWRFAIL\	B	L		Power fail bus signal.
14	DMA3\	M	L	O.C.	Temporary master priority bit 3.
15	A18	M	H		Extended address bit 18.

16	A16	M	H		Extended address bit 16.
17	A17	M	H		extended address bit 17.
18	SDSB\	M	L	O.C.	Disable signal for 8 status lines.
19	CDSB\	M	L	O.C.	Disable signal for 8 control lines.
20	GND	B			Common with pin 100
21	NDEF				Not to be defined. Manufacturer must specify any use in detail.
22	ADSB\	M	L	O.C.	Disable signal for 16 address lines.
23	DODSB\	M	L	O.C.	Disable for 8 data out lines.
24	Φ	B	H		Master timing signal for bus.
25	pSTVAL\	M	L		Status valid signal.
26	pHLDA	M	H		Control signal used in conjunction with HOLD\ to coordinate bus/master transfer operations.
27	RFU				Reserved for future use.
28	RFU				Reserved for future use.
29	A5	M	H		Address bit 5.
30	A4	M	H		Address bit 4.
31	A3	M	H		Address bit 3.
32	A15	M	H		Address bit 15.
33	A12	M	H		Address bit 12.
34	A9	M	H		Address bit 9.
35	DO1/DATA1	M/MS	H		Data out bit 1,bidirectional bit 1.
36	DO0/DATA0	M/MS	H		Data out bit 0,bidirectional bit 0.
37	A10	M	H		Address bit 10.
38	DO4/DATA4	M/MS	H		Data out bit 4,bidirectional bit 4.
39	DO5/DATA5	M/MS	H		Data out bit 5,bidirectional bit 5.
40	DO6/DATA6	M/MS	H		Data out bit 6,bidirectional bit 6.
41	DI2/DATA10	S/MS	H		Data in bit 2,bidirectional bit 10.

42	DI3/DATA11	S/MS	H		Data in bit 3,bidirectional bit 11.
43	DI7/DATA15	S/MS	H		Data in bit 7,bidirectional bit 15.
44	sM1	M	H		Status signal indicating current cycle is op-code fetch.
45	sOUT	M	H		Status signal indicating data transfer bus cycle to output device.
46	sINP	M	H		Status signal indicating data transfer bus cycle from input device.
47	sMEMR	M	H		Status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycles.
48	sHLTA	M	H		Status signal indicating a HALT instruction has been executed.
49	CLOCK	B			2 MHz (0.5%) 40-60% duty cycle. Not required to be synchronous with any other bus signal.
50	GND	B			Common with pin 100.
51	+8 volts	B			Common with pin 1.
52	-16 volts	B			Instantaneous max less than -14.5 volts,instantaneous min greater than -35 volts, average min greater than -21.5 volts.
53	GND	B			Common with pin 100.
54	SLAVE CLR\	B	L	O.C.	Reset signal to reset bus slaves. Must be active with POC\ and may also be generated by external means.
55	DMA0\	M	L	O.C.	Temporary master priority bit 0.
56	DMA1\	M	L	O.C.	Temporary master priority bit 1.
57	DMA2\	M	L	O.C.	Temporary master priority bit 2.
58	sXTRQ\	M	L		Status signal which requests 16-bit slaves to assert SIXTN\.
59	A19	M	H		Extended address bit 19.
60	SIXTN\	S	L	O.C.	Signal generated by 16-bit slaves in response to the 16-bit request signal

					sXTRQ\.
61	A20	M	H		Extended address bit 20.
62	A21	M	H		Extended address bit 21.
63	A22	M	H		Extended address bit 22.
64	A23	M	H		Extended address bit 23.
65	NDEF				Not to be defined signal.
66	NDEF				Not to be defined signal.
67	PHANTOM\	M/S	L	O.C.	Bus signal which disables normal sla devices and enables phantom slaves. Primarily used for bootstrapping systems without hardware front panels
68	MWRT	B	H		Gating of pWR\ - sOUT. Signal must fo pWR\ by no more than 30 ns.
69	RFU				Reserved for future use.
70	GND	B			Common with pin 100.
71	RFU				Reserved for future use.
72	RDY	S	H	O.C.	See comments for pin 3.
73	INT\	S	L	O.C.	Primary interrupt request bus signal.
74	HOLD\	M	L	O.C.	Control signal used in conjuction wit pHLDA to coorodinate bus master trans
75	RESET\	B	L	O.C.	Signal used to reset bus master devic This signal must be active with POC\ and may be generated by external mean
76	pSYNC	M	H		Control signal identifying BSl.
77	pWR\	M	L		Control signal signifying the presenc of valid data on DO bus or data bus.
78	pDBIN	M	H		Control signal that request data on t DI bus or data bus from the currently addressed slave.
79	A0	M	H		Address bit 0.
80	A1	M	H		Address bit 1.
81	A2	M	H		Address bit 2.

82	A6	M	H		Address bit 6.
83	A7	M	H		Address bit 7.
84	A8	M	H		Address bit 8.
85	A13	M	H		Address bit 13.
86	A14	M	H		Address bit 14.
87	A11	M	H		Address bit 11.
88	DO2/DATA2	M/MS	H		Data out bit 2,bidirectional bit 2.
89	DO3/DATA3	M/MS	H		Data out bit 3,bidirectional bit 3.
90	DO7/DATA7	M/MS	H		Data out bit 7,bidirectional bit 7.
91	DI4/DATA12	S/MS	H		Data in bit 4,bidirectional bit 12.
92	DI5/DATA13	S/MS	H		Data in bit 5,bidirectional bit 13.
93	DI6/DATA14	S/MS	H		Data in bit 6,bidirectional bit 13.
94	DI1/DATA9	S/MS	H		Data in bit 1,bidirectional bit 9.
95	DI0/DATA8	S/MS	H		Data in bit 0,bidirectional bit 8.
96	sINTA	M	H		Status signal identifying the bus input cycles that may follow an accepted interrupt request presented on INT\.
97	sWO\	M	L		Status signal identifying a bus cycle which transfers data from a bus master to a slave.
98	ERROR\	S	L	O.C.	Bus status signal signifying an error condition during the present bus cycle.
99	POC\	B	L		Power-on clear signal for all bus devices. During active condition, this signal must stay low for at least 10 msecs.
100	GND	B			System ground bus.