OPERATIONS MANUAL

# Versafloppy II

SD SYSTEMS

OPERATIONS
MANUAL

# VERSAFLOPPY II

# FLOPPY DISK CONTROLLER



JULY 1979

Revision A

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# SECTION I

# GENERAL INFORMATION

## 1-1 INTRODUCTION

VERSAFLOPPY II™ is the new floppy controller board from SD SYSTEMS It features the Western Digital FD1791B-1 double density controller The unique feature of this board is that it may be used with mini or full-size floppy drives, single or double density, single or double sided, in any variation thereof. For example, a mini drive operating single density and a full-size drive operating double density may be utilized at the same time and information may be transferred from one to the other.

VERSAFLOPPY II was designed to be used optimally with SD SYSTEMS' SBC-200, single board computer, and Expandoram boards to form a complete, low cost, disk based computer. The VERSAFLOPPY II is designed for operation with the Z80 CPU and is not recommended for operation with other processors.

## 1-2 GENERAL DESCRIPTION

At the heart of the VERSAFLOPPY II is the powerful Western Digital FD1791B-1 NMOS LSI double density controller chip. This device performs most of the timing and control functions required by floppy disk drives such as:

1. Head load/unload
2. Track seeking with verification
3. Address mark detection/generation
4. Serial to parallel data conversion during reads
5. Parallel to serial data conversion during writes
6. CRC error code checking/generation
7. IBM 3740 Soft Sector compatible reading
8. Signals for double density recording and precompensation

During sector reading and writing, the data rate is synchronized with the CPU by inserting wait states until the FD1791B-1 is ready for the next word.
The VERSAFLOPPY II employs a phase locked loop in the data recovery circuit which insures a valid readback during double density operation.

## 1-3 SOFTWARE CONSIDERATIONS

The control function has been designed to be evenly distributed between the hardware circuit and the control software allowing a great deal of flexibility for the user. A version of the control software is supplied with the VERSAFLOPPY II in listing form configured to run on the SBC-100/200 single board computer. This may be modified to meet the user's specific software interface requirements, such as register usage, parameter hand-offs and data formats.

Also available from SD SYSTEMS is a version of SDOS configured to run on the SBC-100/200, VERSAFLOPPY II and 32K Expandoram II board combination. This allows using several disk based versions of high level languages.

# SECTION II

# FUNCTIONAL DESCRIPTION

## 2-1 INTRODUCTION

Functionally, the VERSAFLOPPY II consists of two main parts: hardware, and the software which controls it. The hardware allows the computer to control the drive selection, head loading, track seeks, formatting, reading and writing operations. The software, as described in Section 3, must direct the hardware in each of these operations. The major functions contained in the VERSAFLOPPY II hardware are shown in the block diagram. (Fig. 2-1) Table 2-1 lists the S-100 Bus signals used by the VERSAFLOPPY II.

## 2-2 FD1791B-1

The FD1791B-1, floppy disk controller chip, performs track to track stepping timing, head load timing, serial to parallel data conversion; parallel to serial data conversion; error code checking/generation, and IBM 3740 softsector compatible recording. After each operation is completed, the chip can optionally interrupt the CPU. (For complete description, see Western Digital FD1791B-1 specification). I/O ports 64,65,66 and 67 are contained within this device.

The FD1791B-1 also has the necessary signals to implement double density operation including a pin to determine whether the chip is to operate single or double density and a late and an early signal for use in precompensation.. The FD1791B-1

has a negative true data bus.

## 2-3 DATA OUT BUS

The 8 bit DATA OUT BUS is the S-100 path for transferring data from the computer (CPU) to the output ports on the VERSAFLOPPY II board.

## 2-4 DATA IN BUS

The 8 bit DATA IN BUS is the S-100 path for transferring data from the input ports on the VERSAFLOPPY II board to the computer (CPU).

## 2-5 A0-A7

The A0-A7 low order eight address lines are used by the computer (CPU) to select the various input/output ports on the board.

## 2-6 I/O CONTROL LINES AND READ/WRITE CONTROL

The I/O Control lines consist of $\overline{\text{PWR}}$, PDBIN, SOUT, SINP. These lines are used to control the input and output operations from/to the I/O ports on the board.

## 2-7 WAIT STATE CONTROL AND PRDY

The Wait State Generator is used by the VERSAFLOPPY II to delay the input and output operations until the FD1791B-1 chip is ready to transfer a word. This PRDY line puts the CPU in a wait state during the delay. Wait states are only generated during sector reads and writes (which use I/O port 67).

## 2-8 ADDRESS DECODER

The Address Decoder detects when a port address used on the VERSA FLOPPY II is present on the low order eight bits of address from the CPU (A0-A7). The output of the decoder is used to gate read and write pulses to the I/O ports.

## 2-9 DATA IN BUFFER

The Data In Buffer isolates the Bi-Directional Data Bus used on the VERSAFLOPPY II from the S-100 Data In Bus. This buffer is enabled during input port reads from ports on the VERSAFLOPPY II. The data is inverted by the Data In Buffer to compensate for the negative true data bus of the FD1791B-1 controller chip.

## 2-10 DATA OUT BUFFER

The Data Out Buffer isolates the Bi-Directional Data Bus used on the VERSAFLOPPY II from the S-100 Data Out Bus. This buffer is enabled except during input port reads from ports on the VERSAFLOPPY II. The output data is inverted by the Data Out Buffer to compensate for the negative true data bus of the FD1791B-1 controller chip.

## 2-11 BI-DIRECTIONAL DATA BUS

The Bi-Directional Data Bus is a path for all transfers to and from the I/O ports on the VERSAFLOPPY II.

## 2-12 INTERRUPT CONTROL

The VERSAFLOPPY II operates with or without interrupts, but the standard control software does not use interrupts.

## 2-13 OUTPUT PORT 63

Output Port 63 is an 8 bit control register with several functions:

1. Bits 0-3 Drive Select 1,2,3,4
2. Bit 4 Side Select for double sided drives
3. Bit 5 5"/8" drives
4. Bit 6 Double/Single density
5. Bit 7 Wait State Enable

## 2-14 INPUT PORT 63

Input Port 63 is used to read the present state of several control signals:

1. Bits 0-7 State of Output Port 63, as described above

## 2-15 SELECT BUFFER

The Select Buffer supplies the current sinking drive for the drive and side select lines.

## 2-16 CONTROL BUFFER

The Control Buffer supplies the current sinking drive for $\overline{\text{WRITE DATA}}$, $\overline{\text{WRITE GATE}}$, $\overline{\text{DIRECTION}}$, $\overline{\text{STEP}}$, $\overline{\text{TRK43}}$, and $\overline{\text{HLD}}$.

## 2-17 SENSE BUFFER

The Sense Buffer receives the $\overline{\text{READ DATA}}$, $\overline{\text{INDEX}}$, $\overline{\text{TRK00}}$, $\overline{\text{READY}}$, and $\overline{\text{WRTPRT}}$ signals from the selected disk drive. Each input is a Schmitt Trigger providing hysteresis noise immunity.

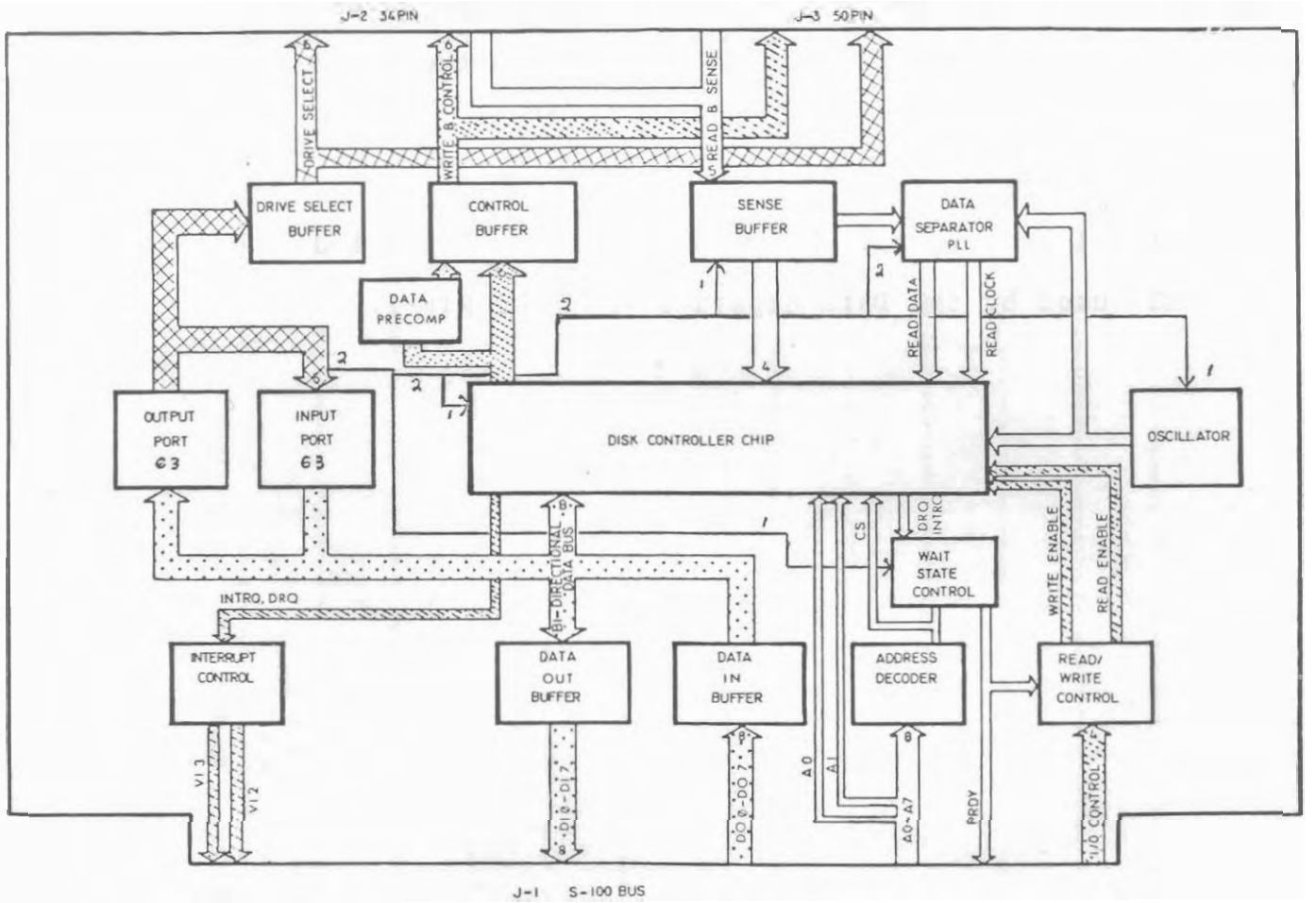
## 2-18 DATA SEPARATOR- PHASE LOCKED LOOP

The Data Separator circuit divides the composite FM & MFM READ DATA

into separated Data and Clock signals required by the FD1791B-1 controller chip. The data separator uses the NE564 phase locked loop circuit to reconstruct the clock from the raw data stream.

## 2-19 OSCILLATOR

The Oscillator circuit provides a crystal controlled squarewave (16MHZ) used by the Data Separator and FD1791B-1.




VERSAFLOPPY II BLOCK DIAGRAM

FIGURE 2-1

TABLE 2-1

S-100 BUS SIGNALS USED BY VERSAFLOPPY II

| PIN | SIGNAL NAME | DIRECTION | DESCRIPTION |
|---|---|---|---|
| 1,51 | +8Volts | | |
| 2 | +16 Volts | | |
| 6 | VI2 | OUTPUT | INTERRUPT CHANNEL 2 (OPTIONAL) |
| 7 | VI3 | OUTPUT | INTERRUPT CHANNEL 3 (OPTIONAL) |
| 24 | Ø2 | INPUT | PHASE 2 CLOCK |
| 25 | Ø1 | INPUT | PHASE 1 CLOCK |
| 29-31, 79-83 | A0-A7 | INPUTS | OW ORDER ADDRESS |
| 35,36,38-40,88-90 | DOØ-DO7 | INPUTS | DATA OUT BUS |
| 41-43, 91-95 | DIØ-DI7 | OUTPUTS | DATA IN BUS |
| 45 | SOUT | INPUT | PORT OUTPUT CYCLE |
| 46 | SINP | INPUT | PORT INPUT CYCLE |
| 72 | PRDY | OUTPUT | READY |
| 77 | $\overline{\text{PWR}}$ | INPUT | WRITE |
| 78 | PDBIN | INPUT | DATA BUS IN |
| 99 | $\overline{\text{POC}}$ | INPUT | POWER ON CLEAR |
| 100,50 | GROUND | | |

# SECTION III

# CONTROL SOFTWARE

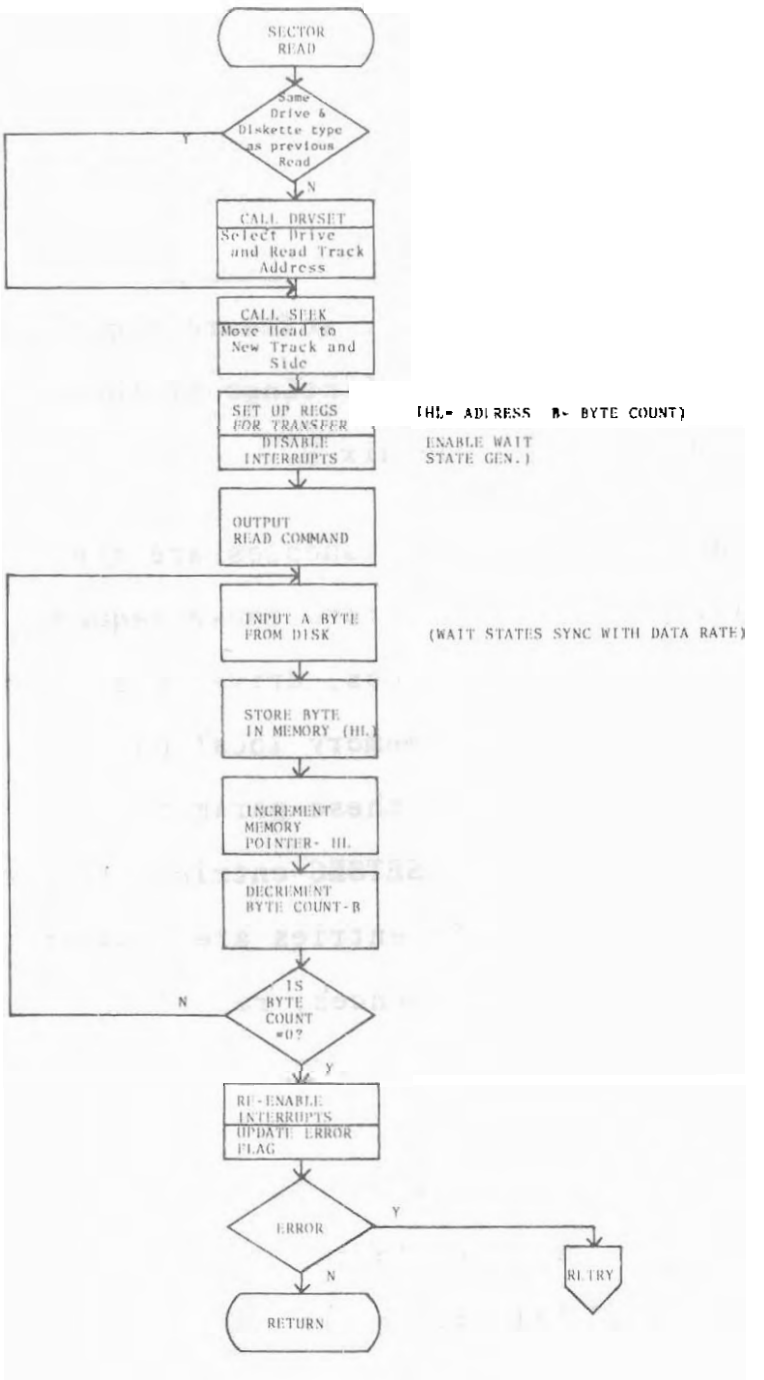
## 3-1 INTRODUCTION

The versatility of the VERSAFLOPPY II is maintained by its ability to be controlled by software. Certain sequences must be executed to ensure proper operation of the disk drive. These control sequences are supported by the SD SYSTEMS' DDBIOS software program. This section will cover these basic software sequences with verbal and graphic description. Program listings of the software in Z-80 source code are included in Appendix E.

The SECTOR READ and SECTOR WRITE sequences are the two main entries into the controlling software. Before these sequences may be entered, the memory transfer address, drive select, track, and sector must have been stored in memory locations. When operating with SDOS Disk Operating System, these parameters are set up when the SETDMA, SELDSK, SETTRK, and SETSEC entries, respectively, are called. The READ and WRITE SDOS entries are linkages to the SECTOR READ and SECTOR WRITE sequences, respectively. If an error is encountered in the Read or Write process, two more attempts will be made to execute the process. After this a Reseek will be executed and then three more Retrys. If an error still exists, program control will be returned to the user with the Z bit reset. If no error exists the Z bit will be set upon Return.

## 3-2 SECTOR READ SEQUENCE (Figure 3-1)

The function of the SECTOR READ SEQUENCE is to do everything necessary to transfer the previously specified sector (128 BYTES) to the previously specified memory buffer (anywhere in the system RAM):




SECTOR READ SEQUENCE

FIGURE 3-1

The unit byte is compared to the unity check byte to determine if the desired drive and diskette type is the same as the previously selected drive and diskette type. If not, the DRVSET routine is called to set up the new drive and determine the diskette type table address to be stored in the IX index register. If DRVSET is called then ID READ is also called to set up the track address of the new drive.

The SEEK and TRINT (section 3-5) subroutines are called to put the Read/Write head on the requested side and track.

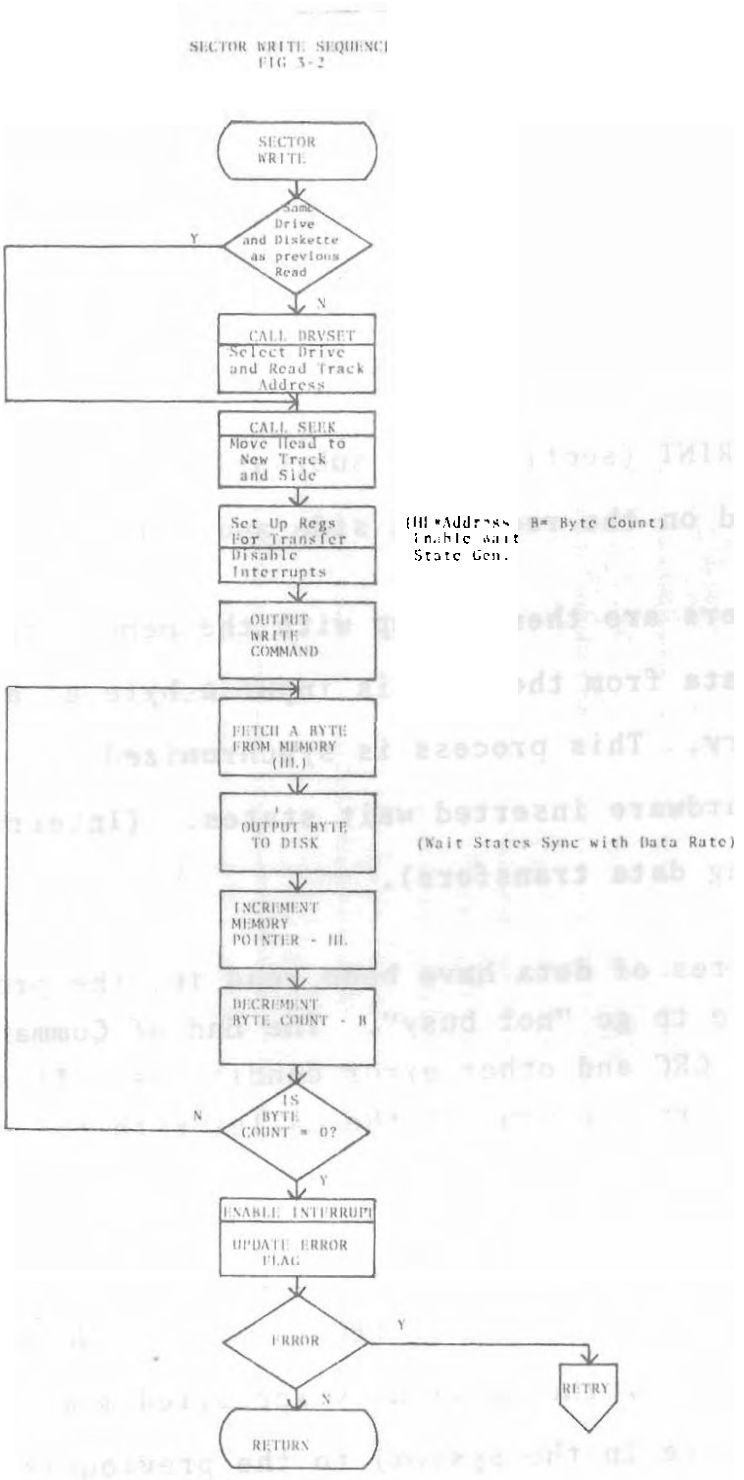
The CPU registers are then set up with the memory address and byte count. Data from the disk is input a byte at a time, and stored in memory. This process is synchronized with the disk data rate by hardware inserted wait states. (Interrupts are disabled during data transfers).

When all 128 bytes of data have been read in, the program waits for the hardware to go "not busy". The End of Command Routine then checks for CRC and other error conditions. If no errors occured, the program returns to the caller with the error flag cleared.

## 3-3 SECTOR WRITE SEQUENCE (figure 3-2)

The function of the SECTOR WRITE SEQUENCE is to do everything necessary to transfer the previously specified memory buffer (128 bytes anywhere in the system) to the previously specified disk sector.

The unit byte is compared to the unit check byte to determine if the desired drive and diskette type is the same as the previously




SECTOR WRITE SEQUENCE

Figure 3-2

selected drive and diskette type. If not, the DRVSET routine is called to set up the new drive and determine the diskette type table address to be stored in the IX index register. If DRVSET is called then ID READ is also called to set up the track address of the new drive.

The SEEK and TRINT (section 3-5) subroutines are called to put the Read/Write head on the requested side and track.

The CPU registers are then set up with the memory address and byte count. The data is output a byte at a time, to the disk. This process is synchronized with the disk rate by hardware inserted wait states. (Interrupt are disabled during data transfers).

When all 128 bytes of data have been output, the program waits for the hardware to go "not busy". The End of Command Routine then checks for CRC and other error conditions. If no errors occurred, the program returns to the caller with the error flag cleared.

## 3-4 DRIVE SELECTION SEQUENCE (Figure 3-3)

The DRIVE SELECTION SEQUENCE translates the data in the unit byte into the format of the select register. The IX index register is then set up with the diskette type table address desired. The new selection is output followed by a delay for Drive Select. This delay is 18 milliseconds for a full-size drive and about 50 milliseconds for a mini.

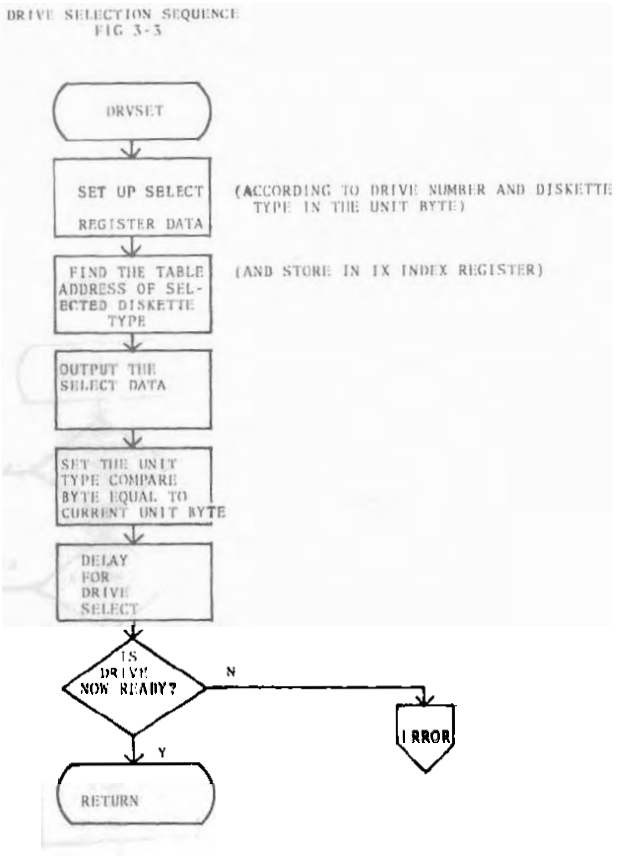
The status is then read to verify that the drive is ready. If the drive is not ready, the error exit is taken.

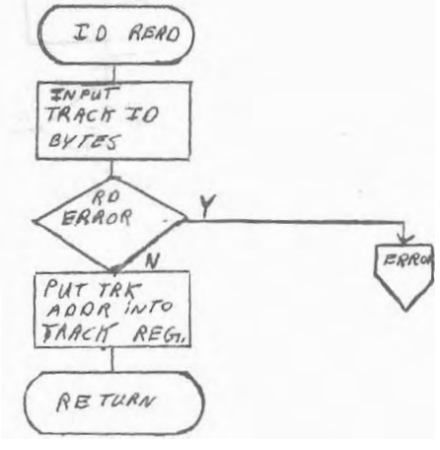
### ID READ

In the ID READ ROUTINE the track address is read from the disk to inform the hardware of what track the new drive's read/write head is presently on. The normal return routine is then executed.

## 3-5 TRACK SEEK AND TRANSFER INITIALIZATION

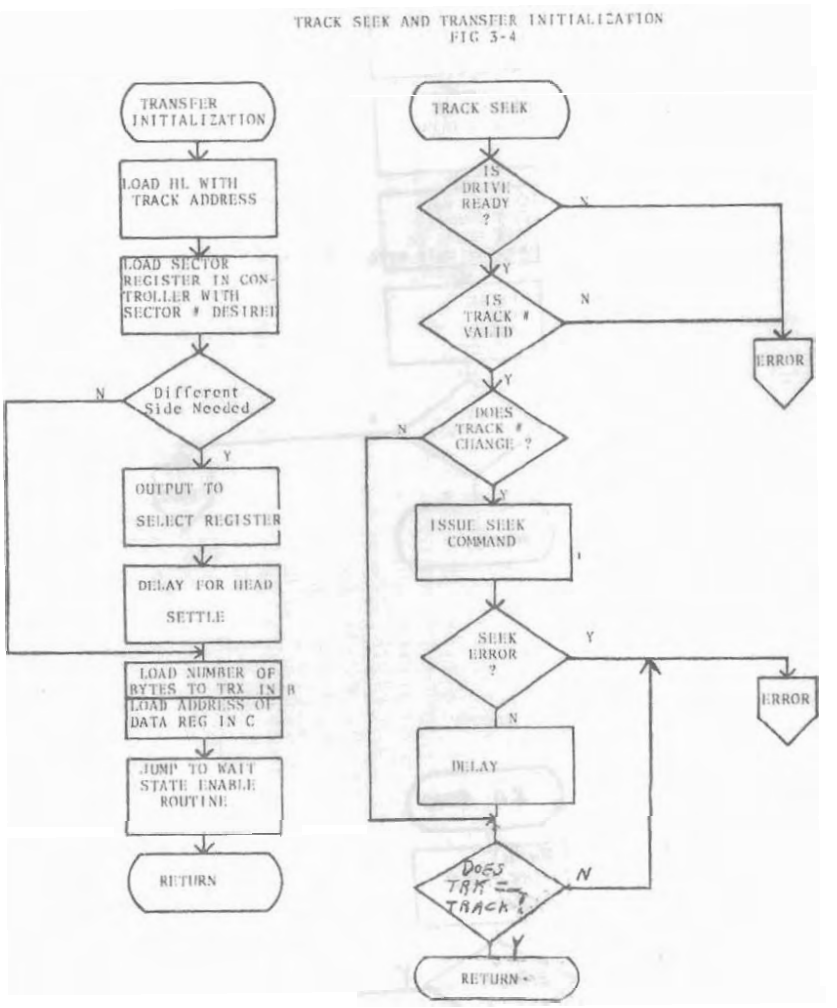
The TRACK SEEK routine moves the head to the proper track, after verifying the track is valid. The TRANSFER INITIALIZATION (TRINT) sequence is responsible for verifying that the requested sector is a valid number and in the case of the double-sided drives, select the proper side of the disk. The Transfer Address is also set up in this routine.




DRIVE SELECTION SEQUENCE

Figure 3-3



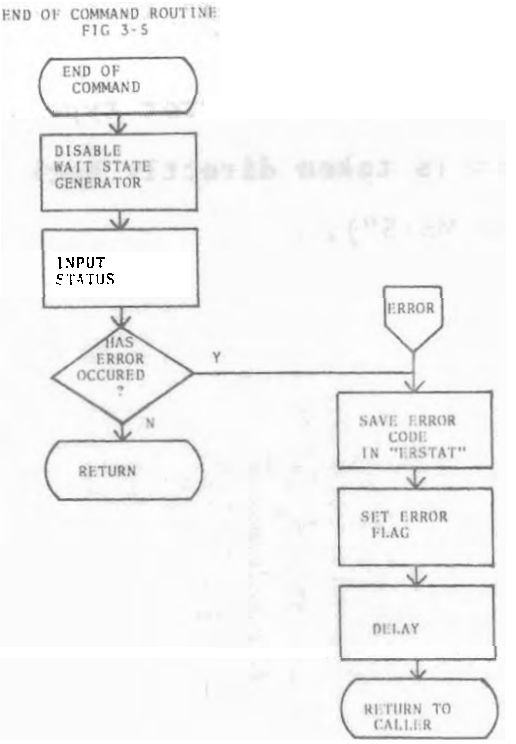

TRACK SEEK

Figure 3-4

## 3-6 END OF COMMAND ROUTINE (figure 3-5)

The END OF COMMAND ROUTINE is entered after both normal and error terminations of hardware executed commands. The routine waits for the FD1791B-1 to become "not busy". The wait state generator is then disabled, and the status is input to check for errors. If no error occurred, then a normal return is taken.

If an error condition is detected, the error type is saved, error flag set and a return is taken directly back to the caller after a delay (18 MS-8"; 50 MS-5").




END OF COMMAND ROUTINE

Figure 3-5

# SECTION VI

# SOFTWARE OPTIONS

## 6-1 INTRODUCTION

The standard control software for the VERSAFLOPPY II is supplied in listing form (Appendix D) and also available in 2716 PROM for an additional charge. This software is called DDBIOS (Double Density Basic I/O System) and is assembled to reside at F000H.

## 6-2 BOOTING UP THE SDOS

In order to run SDOS, a minimum of 16K of RAM must be in the system starting at address 0000 and the BIOS PROM must be at F000H. Execute BIOS at F000 and SDOS will be booted and promp with "[A]". Refer to the "SD SYSTEMS DISK OPERATING SYSTEM (SDOS) USER'S GUIDE" for details of the SDOS commands.

# SECTION VII

# CHECK - OUT

## 7-1 INTRODUCTION

This section will describe some basic checks that should be made on the VERSAFLOPPY II. NOTE: It is assumed at this point that the voltage checks described in Section 4 have been previously made. The following checks require that the CPU board also be plugged into the Bus.

## 7-2 OSCILLATOR

Apply power to board and verify that there is a 16MHZ clock on U3 - Pin 2.

## 7-3 $\overline{RE}$ AND $\overline{WE}$ PULSES

Verify that U10 Pin 4 pulses low during any Input instruction, and U10 Pin 2 pulses low during any output instruction.

## 7-4 I/O PORT WRITE/READ VERIFICATION

Using the monitor in the system or a short program, write data to port 65 and read it back. Verify that the data read back is the same as that written. This is done to test the data path to and from the FD1791B-1 as well as the internal register. REPEAT this procedure for ports 66, 67 and 63.

## 7-5 HEAD LOAD MONOSTABLE

After the diagnostic software is operating, check U20-Pin 3 for a 35 millisecond pulse (low) and U20-Pin 2 for a 1.5 sec pulse (low) each time the head loads.

## 7-6 PHASE LOCKED LOOP FINAL ADJUSTMENT

In order to fine tune the data separator for best performance, the following procedure should be followed:

1. Execute the Read Test using VDFIAG (section VIII) on a previously formatted diskette. (Use double density Read and Format type codes)
2. While listening to the step rate of the Drive adjust C3 slightly clockwise until hesitation begins to occur. Then adjust counter clockwise until hesitation again occurs.
3. Set C3 adjustment in the middle of the range in step 2.
4. Allow test to run one full sweep through diskette. If hesitation occurs make very slight adjustments to minimize the hesitation.
5. After above adjustments the test should run with no error printouts.

# SECTION VIII

# DIAGNOSTIC SOFTWARE

## 8-1 INTRODUCTION

A diagnostic program for the VERSAFLOPPY II is supplied in the top of the 2716 DDBIOS PROM. The diagnostic program is also on the diskette, when SDOS is purchased, under the file name of "VFDIAG.COM" Once SDOS is operating, the diagnostic may be run by typing VFDIAG (CR). THE SDOS DISKETTE SHOULD NOT BE PLACED IN THE DRIVE UNTIL THE VERSAFLOPPY II AND DISK DRIVES HAVE BEEN THOROUGHLY CHECKED OUT.

When running the diagnostic to check-out the VERSAFLOPPY II, execute the program starting at address F600. The diagnostic uses the DDBIOS and monitor PROMS for disk and console I/O.

## 8-2 DIAGNOSTIC TEST START-UP

Upon executing the diagnostic program the following message will print on the console:

TEST# DRV# (TTDD)

The program then waits for the test number and drive number to be entered from the console followed by a carriage return.

NOTE: The test number and drive number are each two digits and MUST NOT be separated by a comma or space. Table 8-1 shows drive numbers.

| Type / Drive | #Sides Disk Size Density | 1 Full Single | 2 Full Single | 1 Mini Single | 2 Mini Single | 1 Full Double | 2 Full Double | 1 Mini Double | 2 Mini Double |
|---|---|---|---|---|---|---|---|---|---|
| A | | 00 | 10 | 20 | 30 | 40 | 50 | 60 | 70 |
| B | | 01 | 11 | 21 | 31 | 41 | 51 | 61 | 71 |
| C | | 02 | 12 | 22 | 32 | 42 | 52 | 62 | 72 |
| D | | 03 | 13 | 23 | 33 | 43 | 53 | 63 | 73 |

TABLE 8-1

Note that these unit numbers must also be used with R, W and Z commands in the SD Monitor.

The test routines (except for 05) may be terminated at any time by entering a period (.) on the console keyboard. The diagnostic will then print the above prompting message and wait for further keyboard entries. If the period (.) is entered instead of a command, control will be transferred to the monitor.

## 8-3 DIAGNOSTIC TEST 00 (SEEK TEST)

Test 00 is a simple routine to verify that the VERSAFLOPPY II is receiving commands properly and that the track seek circuitry is functional. The selected drive should begin moving the head from track 00 to the inside track (76 for full size, 34 for mini) and back again. Enter a period on the keyboard to cause the test to cease.

## 8-4 DIAGNOSTIC TEST 01 (WRITE/READ)

Diagnostic test 01 writes random data on each sector, reads the

sector back and compares the data to verify that it is identical. Any errors which occur will be printed on the console. (see Section 8) This is done to each sector sequentially, starting at track 00, sector 1, until reaching the innermost track. At that point it prints a "P" on the console, returns to track 00, and continues.

NOTE: Diagnostic tests which read and write to disk may only be run after the diskette has been formatted using diagnostic 05. (see 8-8)

## 8-5 DIAGNOSTIC TEST 02 (READ TEST)

Test 02 reads every sector on the disk sequentially and checks for CRC errors, and seek errors. Errors will be reported on the console. This test should step from track to track at the same rate as when formatting a diskette.

## 8-6 DIAGNOSTIC TEST 03 (RANDOM WRITE/READ)

This test is similar to test 01 in that it writes, reads and compares data byte by byte. However, test 03 chooses the sectors and tracks on a random basis in an attempt to simulate actual use. This test exercises only on the specified drive.

## 8-7 DIAGNOSTIC TEST 04 (MULTI-DRIVE RANDOM WRITE/READ

This test is identical to test 03 except that it also selects a random drive (0 or 1).

## 8-8 DIAGNOSTIC TEST 05 (FORMATTING)

Test 05 is actually not a diagnostic, but a program which formats a diskette in accordance with drive and density type. This must be done to all diskettes before further use. Note that on the distributed SDOS diskette there is a program which formats a diskette. This program has the filename "FORMAT.COM" and may be run by entering "FORMAT (CR)". BE SURE TO USE A SCRATCH OR UNFORMATTED DISKETTE WHEN FORMATTING BECAUSE ANY PREVIOUSLY WRITTEN DATA WILL BE LOST.

## 8-9 DIAGNOSTIC TEST FF (JUMP)

Test code FF allows exiting the diagnostic to anywhere in memory. The following sequence describes this:

| CONSOLE INTERACTION | COMMENTS |
|---|---|
| TEST # DRV # (TTDD): FF00 (CR)<br>ADDRESS: 3000 (CR) | Jump to address 3000H |

## 8-10 DIAGNOSTIC ERROR REPORTING

If any errors occur during diagnostics 1,2,3, or 4, the errors will be reported on the console as follows:

```
CMD STAT DRV TRK SCTR CC SS DD TT SS
```

where CC = The controller command being executed
SS = The error status (type of error)
DD = The drive being tested
TT = The track being tested
SS = The sector being tested

Table 8-1 lists all the various controller commands and Table 8-2 contains the definition of each bit in the error status byte.

TABLE 8-1

DISK CONTROLLER COMMAND CODES

| MINI DISK CMD CODE | FULL SIZE CMD CODE | DESCRIPTION |
|---|---|---|
| 0B | 09 | Restore Drive TRK ØØ |
| 13 | 19 | Track Seek with No Verify |
| F4 | F4 | Format Track |
| 88 | 80 | Read Sector |
| A8 | AØ | Write Sector |
| C4 | CØ | Read Track Address |

TABLE 8-2

ERROR STATUS DEFINITION

| BIT # | DEFINITION |
|---|---|
| BIT Ø | Busy |
| BIT 1 | DRQ Bit (Indicates Excessive noise on S-100 Bus) |
| BIT 2 | Data Lost |
| BIT 3 | CRC Error |
| BIT 4 | Sector Not Found |
| BIT 5 | Track Seek Error |
| BIT 6 | Write Protected Diskette |
| BIT 7 | Drive Not Ready |
| FE | Controller Hang Up |
| ØF | Invalid, Track Error |

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# ADDENDUM VERSAFLOPPY II
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The following changes must be noted when assembling the Versafloppy II Kit.

1) R 12 is a 100 K OHM resistor.
2) You must add a 330 pf. cap to GND from pin 38 end of R12.
3) You must add a 47K OHM resistor to ground from pin 1 of U10.

Note: If the board in your kit is REV. C (see the silk screen on the board) the following changes must also be made.

4) Cut the etch between pins 3 and 4 of IC U3.
5) Add jumpers between pins 14, 3, 7 and 10.

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# ADDENDUM VERSAFLOPPY II
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Page 1, 1-1
The second paragraph should be followed by:
The versafloppy II is designed for operation with the Z-80 CPU and is not recommended for operation with other processors.

Page 6, 2-18
The letters PPL stand for Phase Locked Loop.

Page 10, 3-2
The last sentence of the first paragraph should read as follows:
"The SEEK and TRINT (section 3-5) subroutines are called to put the read/write head on the requested side and track."

Page 11, 3-3
The last sentence of the second paragraph should read as on page 10(see above).

Page 16, 4-4
Delete item 4

Page 18, 6-1
This paragraph should read as follows:
The standard software for the Versafloppy II is supplied in listing form (Appendix D) and also available in 2716 PROM for an additional charge. This software is called DDBIOS (Double Density Basic I/O System) and is assembled to reside at F000H.

Page 20
Add 7-6 to read as follows:
In order to fine tune the Data Separater for best performance the following procedure should be followed.
1) Execute the read test using VFDIAG (Section VIII) on a previously formatted diskette.(Using Double Density Read and format type codes)
2) While listening to the step rate of the drive, adjust C3 slightly clockwise until hesitation begins to occur. Then adjust counter-clockwise until hesitation again occurs.
3) Set C3 adjustment in the middle of the range in Step 2.
4) Allow test to run 1 full sweep through diskette. If hesitation occurs make very slight adjustments to minimize the hesitations.
5) After above adjustments the test should run with no error printouts.

Page 21, 8-1
The last sentence should read as follows:
The diagnostic uses the DDBIOS and monitor PROMS for disk and con-

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sole I/O.

Page 22, 8-2
After the last sentence add the following:
If the Period(.) is entered instead of a command, control will be transferred to the monitor

Page 23, 8-4
Delete the last sentence.

Page 24,8-8
This paragraph should read as follows:
Test 05 is actually not a diagnostic, but a program which formats a diskette in accordance with drive and density type. This must be done to all diskettes before further use. Note that on the distributed SDOS diskette there is a program which formats a diskette. This program has the filename "FORMAT.COM" and may be run by entering "FORMAT (CR)". BE SURE TO USE A SCRATCH OR UNFORMATTED DISKETTE WHEN FORMATTING A DISKETTE BECAUSE ANY PREVIOUSLY WRITTEN DATA WILL BE LOST.

Page 25, Table 8-1
Delete lines 5 & 7. Line 8 changed.

TABLE 8-1

DISK CONTROLLER COMMAND CODES

| MINI DISK CMD CODE | FULL SIZE CMD CODE | DESCRIPTION |
|---|---|---|
| 0B | 09 | Restore Drive TRK ØØ |
| 13 | 19 | Track Seek with No Verify |
| F4 | F4 | Format Track |
| 88 | 80 | Read Sector |
| A8 | AØ | Write Sector |
| C4 | CØ | Read Track Address |

Please see the revised pages attached.