EXPANDORAM IV

OPERATIONS MANUAL

SD #7140173
REVISION C
NOVEMBER 3, 1983

SDSYSTEMS
A SYNTECH COMPANY

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TERMINATION NOTE

SDSystems recommends the use of active termination circuitry on the S-100 bus to avoid system problems.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

ILLUSTRATION

TABLES

SECTION I
INTRODUCTION

1.0 GENERAL

The SDSystems EXPANDORAM IV board is a high performance memory board meeting the IEEE-696 bus specifications. The EXPANDORAM IV can be configured as either a parity detection board or an Error Detection and Correction (EDC) board. The board contains either 256K or 1Mbyte of memory depending upon the configuration.

The EXPANDORAM IV uses the Intel 8207 Dynamic RAM controller and the Intel 8206 EDC chips as the heart of the board. These chips operate asynchronously to the system clock and perform all the necessary timing and arbitration to interface the IEEE-696 bus signals to the Dynamic RAM chips.

1.1 FEATURES

The EXPANDORAM IV board provides a low cost means for expanding Random Access Memory (RAM) capability for computers utilizing the IEEE-696 S-100 bus structure. The EXPANDORAM IV operates asynchronously at 5, 8 or 16 mHz, and either an on-board timer or bus OP CODE fetches can be used for refresh.

The EXPANDORAM IV board uses NMOS dynamic memory devices and may be configured to have a memory capacity of 256K bytes (64Kx1 DRAMs) or 1 Mbyte (256Kx1 DRAMs).

Additional features:

* Phantom memory disable.
* Typical power dissipation of 15 watts.
* 5, 8 or 16 mHz asynchronous operation.
* Port addressable bank select for multi-user system.
* Parity check using a parity bit for each 8-bit byte of memory.
* Error Detection and Correction (EDC) for correcting single bit errors and reporting multi-bit errors.

* Support of both 8 and 16 bit data transfers from any permanent or temporary bus master.

* Support of 24 bit addressing capability of the IEEE-696 bus.

* Variety of RAM chip speeds determined by number of wait states inserted in memory cycles.

1.2 SCOPE

This document describes the function, performance, electrical and physical characteristics of the EXPANDORAM IV memory subsystem. For detailed descriptions of individual integrated circuits, consult the manufacturer's data sheets.

SECTION II
FUNCTIONAL DESCRIPTION

2.0 GENERAL

This section provides a functional description of the basic blocks which make up the EXPANDORAM IV memory board. A block diagram of the EXPANDORAM IV appears in Figure 2-1.

The EXPANDORAM IV communicates with the IEEE-696 bus asynchronously by asserting the RDY line, when the board is accessed, until the 8207 Advanced Dynamic RAM Controller (ADRC) responds with an acknowledge (XACK) signal. The XACK signal informs the board that data has been read or written and is available to the system. The board then releases the RDY line and waits for the next access.

2.1 RAM (MEMORY) ARRAY

The memory array consists of either 36 or 44 RAM chips depending on whether the board is configured as parity or EDC. The RAM is organized as two banks of 18 (22) chips in a 2x9 (2x11) matrix. The matrix is two 9 (11) bit words composed of an 8 bit data byte and 1 parity (3 syndrome) bit. The bank consists of two 11 bit words to facilitate the EDC mode.

The 8206 EDC chip uses a modified Hamming code which requires 6 syndrome bits for a 16 bit word or 5 bits for an 8 bit word. The 16 bit approach was chosen to save memory. Therefore, whether the system is doing 8 or 16 bit transfers, the memory board always performs 16 bit reads and writes when in the EDC mode. However, this 16 bit transfer is transparent to the system bus and/or user.

2.2 RAM CONTROLLER (8207)

The Intel 8207 Advanced Dynamic Ram Controller (ADRC) is the heart of the EXPANDORAM IV board and controls all the interface and timing with the Dynamic RAM chips. The ADRC also controls the 8206 EDC chip, when in the error correction mode.

The ADRC arbitrates between memory accesses and refresh requests to decide priorities. The ADRC features a refresh interval counter which allows refresh to be totally controlled by the chip and to be transparent to the user.

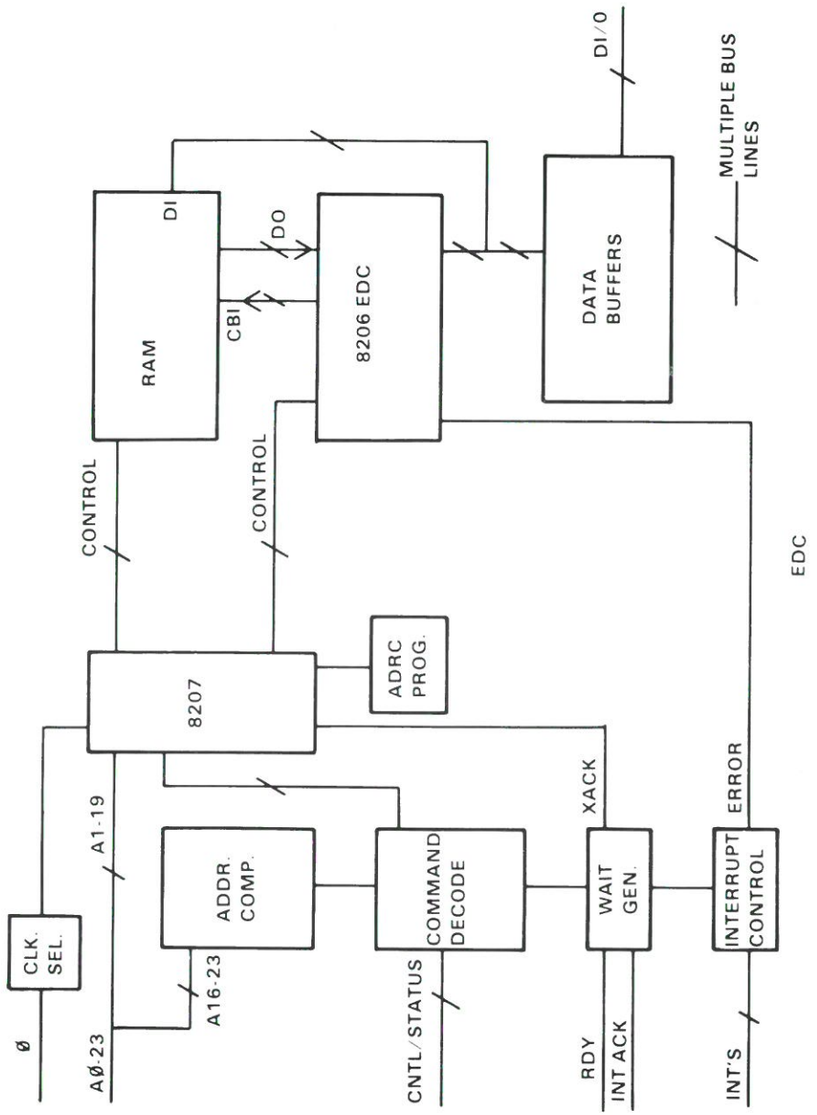

Figure 2-1. BLOCK DIAGRAM (Sheet 1)

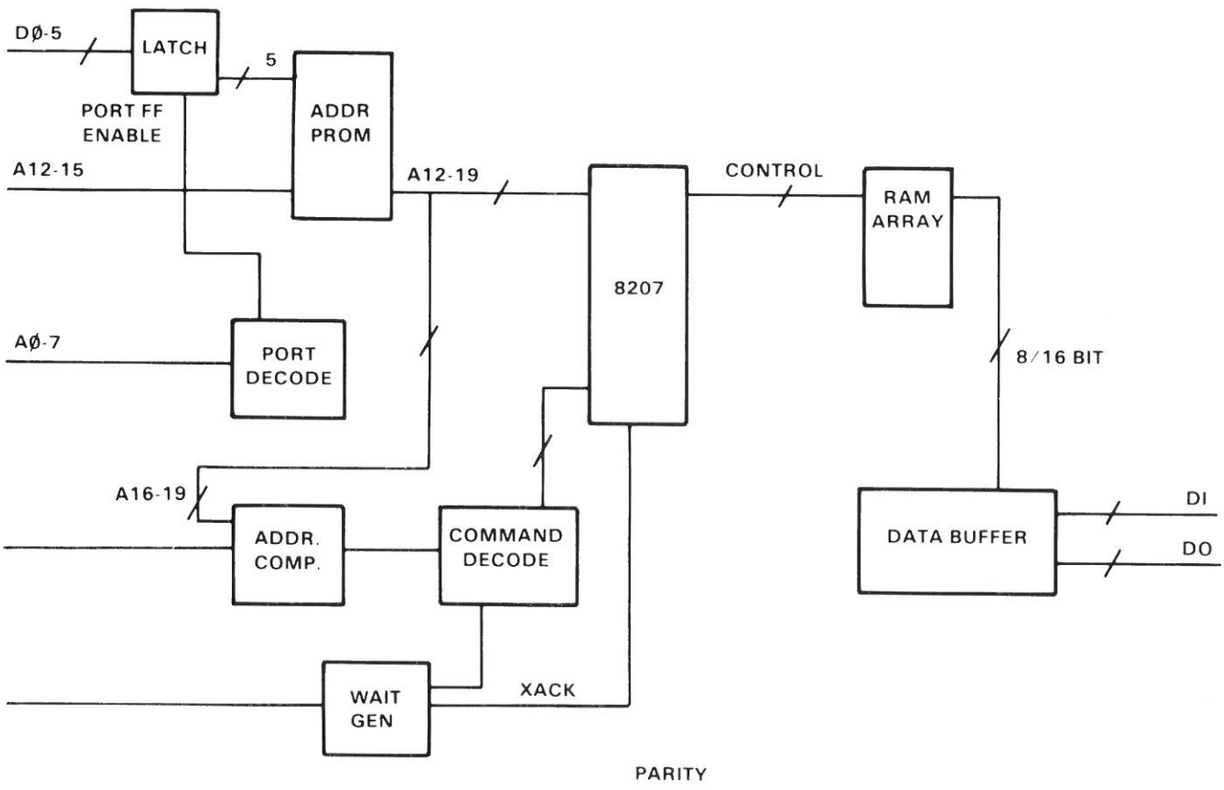

Figure 2-1. BLOCK DIAGRAM (Sheet 2)

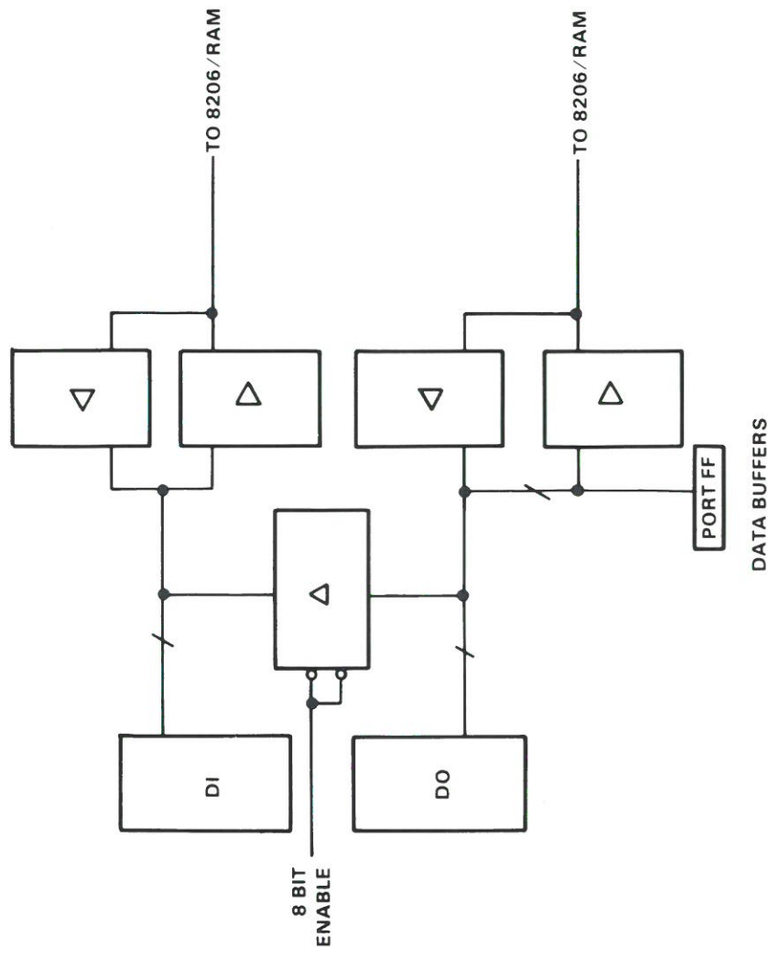

Figure 2-1. BLOCK DIAGRAM (Sheet 3)

The ADRC must be programmed at initialization and the user has the option of changing any of the factory options.

2.3 ERROR DETECTION AND CORRECTION

The Intel 8206 EDC chip is used in conjunction with the 8207 ADRC to provide complete one bit error detection and correction and two bit error detection. The chip set uses a modified Hamming code. The chip set operates asynchronously to the bus and places the system in a wait state while a memory cycle is in process. This is necessary because the chip set must synchronize timing with the system and wait for the error checking to be completed.

2.4 DATA BUFFERS

The data buffer section is responsible for properly gating data from or to the bus and to the memory array. The data buffers are switched for eight or 16 bit transfers by monitoring the sXTRQ* (16 request) signal. When this signal is active, data transfers will be 16 bit; otherwise transfers will be eight bit.

2.5 ADDRESS COMPARATOR

The address comparator compares the high order address bits (A16-A23) with the selected board starting address (256K or 1Mbyte boundaries depending on board size) and activates the board select line if there is a match.

2.6 COMMAND DECODER

The command decoder is a 20L10 PAL and associated circuitry. The decoder monitors the bus status signals and board select. When the board is accessed, the decoder decides what type of access is requested, activates the wait state generator, and outputs the control signals to the controller chip and buffers.

2.7 WAIT STATE GENERATOR

The EXPANDORAM IV board is an asynchronous memory board and must match the bus timing to be able to transfer data. Therefore, after a board access is decoded, the wait state generator is activated until either the transfer acknowledge (XACK) signal from the 8207 or a reset clears the wait. The XACK signal signifies the completion of the memory cycle and lets the bus continue.

2.8 INTERRUPT CONTROL

The interrupt control section allows the user to jumper an error condition (parity or noncorrectable error) to one of the vectored interrupt lines, to the error line, or to the NMI line. An LED is latched on when a noncorrectable error is found.

2.9 ADRC PROGRAMMING

The 8207 has a 16 bit program data word which must be configured before power-on to allow proper operation. The word is programmed by jumpers W7 and W10. After reset, these bits are shifted into the 8207 using the external shift registers.

2.10 CLOCK SELECT

This section contains the on-board clock oscillator circuitry and a clock select jumper to choose between the on-board clock and the bus clock. The on-board oscillator can be 5, 8 or 16 mHz depending on the chip speeds and mode of operation. In general, the faster the clock speed, the shorter the memory cycle time and thus the faster the board speed.

2.11 PARITY MODE

When the board is set up as a parity only board, the 8206 chip is deleted and 8 extra RAM chips are deleted. Several jumper changes and programming changes are required to complete the change.

2.12 BANK SELECT MODE

The EXPANDORAM IV supports bank or page select in addition to extended addressing. If bank select mode is chosen, the user must write to I/O port FF to select the user number before trying to access a given page. The board latches the user number and uses it along with address lines A12-A15 to create on-board addresses. The bank select PROM selects 48K user pages and 16K of common area. The 256K board has space for 5 users.

2.13 HOST MEMORY MAP SELECTION

The EXPANDORAM IV may occupy any 256K (using 64K byte DRAMs) or 1Mbyte (using 256K byte DRAMs) block of IEEE-696 memory space. S1 is an 8 position dip switch used to select which block the board will occupy. The IEEE-696 bus supports 24 bits of memory address (000000H-FFFFFFH).

For 256K byte EXPANDORAM IV boards, S1-1 through S1-6 select the 256K block. These 6 switch positions are compared to bus address A18-A23 to determine if this board is being addressed (switch positions: ON's are 0's and OFF's are 1's). S1-7, 8 must be left "OFF" for 256K byte EXPANDORAM IV boards.

For 1Mbyte EXPANDORAM IV boards, S1-1 through S1-4 select the 1Mbyte block. These 4 switch positions are compared to bus address A20-A23 to determine if this board is being addressed. S1-5, 6, 7, 8 must be left "OFF" for 1Mbyte EXPANDORAM IV boards.

SECTION III
THEORY OF OPERATION

3.0 GENERAL

The EXPANDORAM IV is an advanced Dynamic RAM memory board with the option of having EDC or parity. The board can supply the necessary signals to address, refresh, and directly drive 64K or 256K Dynamic RAMs.

The 8207 Advanced Dynamic RAM Controller (ADRC) can insert synchronization circuitry into read (RD*), write (WR*), port enable (PE*), and port control (PCTL) inputs to allow the board to operate at 8 or 16 mHz and asynchronously to the system bus.

3.1 CIRCUIT ANALYSIS

Starting on the left side of page 3 of the EXPANDORAM IV schematic (see Schematic Appendix), a read or write cycle is begun by applying the address. The upper 8 address bits are compared to the board address by U28 (74LS682). If a match is made, the board select (BRDSEL*) signal is generated. The occurrence of a BRDSEL* signal and a memory read or write will cause a MEMSEL* signal which will deassert the RDY line to the host processor.

Simultaneous with creating the MEMSEL*, the board will create either a RDCMD* (read command) signal or a WRCMD* (write command) signal which activates the proper command sequence with the 8207.

The host will stay in this wait state until the ADRC has completed the memory access and returned the transfer acknowledge (XACK*) signal.

3.1.1 Read Process

The sMEMR signal will be asserted during a memory read cycle.

The sM1 status line is the OP CODE fetch signal and signifies that the master is fetching an instruction from the bus. Depending on the implementation of a particular master, this line may also be active during an interrupt acknowlege cycle.

The signal pDBIN is a read strobe from the master. It is asserted for all read cycles and is used by the EXPANDORAM IV in U24 so that the data to be read is gated onto the bus at the proper time.

In order for the RDCMD* to be generated, the proper address must be on the bus so that a BRDSEL* can be generated from U28 (74LS682, 8 bit comparator). RDCMD* is generated by the simultaneous occurrence of BRDSEL*, sMEMR, pDBIN, and PHANTOM*.

The XACK* signal is asserted by the 8207 at the completion of the memory cycle to inform the system that the read has been completed and to clear the wait state.

3.1.2 Phantom Signal

This signal is provided so that the EXPANDORAM IV may exist in the same address space as another device by the two overlying one another. One device (the phantom) is inactive if PHANTOM* is inactive and a normal device is active. When PHANTOM* is asserted, the phantom device becomes active and the normal device becomes inactive.

3.1.3 Write Process

During the write cycle, the monitor transfers data to the EXPANDORAM IV. The 2 types of write cycles are memory write and I/O write. The differences are that during a memory write cycle the address bus may contain 16 or 24 bits of information and the status bus will reflect a memory write cycle, while during an I/O write cycle the address bus may contain 8 or 16 bits of information and the status bus will reflect an I/O write cycle. In addition the strobe MWRT will be asserted during a memory cycle but not during an I/O cycle.

For generation of WRCMD*, first BRDSEL* must be generated from the proper address being applied to U28 (8 bit comp.). The signal is transferred to U24 for generation of WRCMD*. WRCMD* is generated by the simultaneous occurrence of sOUT*, sINP*, pWR, sWO, MWRT, and PHANTOM*.

After the WRCMD* signal is asserted, the 8207 enters a write cycle and writes the data into the correct memory location. At the completion of the cycle, XACK* is asserted to clear the wait state.

3.2 EDC

The error detection and correction on the EXPANDORAM IV board is provided by an 8206 EDC chip from Intel. It is a single chip device which can detect and correct all single bit errors and detect all double bit and some higher bit errors. The error handling is a function of the number of check bits used and the specific Hamming code. The Hamming code for a 16 bit word uses 6 syndrome bits. Decoding the syndrome bits can tell the user the specific location or type of error found by the 8206. (See Table 3-1.)

Table 3-1. SYNDROME DECODING

Syndrome Bits																	
		3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
5	4																	
0	0		N	CB0	CB1	D	CB2	D	D	X	CB3	D	D	0	D	1	2	D
0	1		CB4	D	D	5	D	6	7	D	D	3	X	D	4	D	D	X
1	0		CB5	D	D	11	D	X	12	D	D	8	9	D	10	D	D	X
1	1		D	13	14	D	15	D	D	X	X	D	D	X	D	X	X	D

N - No error
CBX - Error in check bit X
D - Double bit error
X - Not defined for 16 bits

SECTION IV
OPERATIONS

4.0 GENERAL

The EXPANDORAM IV can be configured to operate with different speed processors and different size and speed RAM chips. The versatility afforded by these options requires that the board be programmed for the particular RAMs and processors with which it will be used.

4.1 OPTIONS

4.1.1 Host CPU Options

Three jumpers are available to tailor the EXPANDORAM IV board to a specific hardware configuration. Jumper W21 allows the 16 request (sXTRQ*) signal to be pulled high for processors which do not meet the IEEE-696 specification (SDSystems SBC-200). Jumper W22 is a write select jumper for non-IEEE-696 boards. It allows either the sWO* signal or the inverted sMEMR signal to be used by the PAL for command generation (the SBC-200 does not generate sWO* and must use inverted read [not read]). Jumper W23 selects which read signal the PAL uses for generation of the on-board read command. It selects either sMEMR or pDBIN.

4.1.2 Memory Size Selection

Memory size selection determines which type of RAM chips (64K/256K) the board will support. Jumpers W1 and W3 connect the extra address bits to the two RAM banks for 256K RAMs. Jumper W12 determines which address bits get to the address comparator for size selection. The 1Mbyte board is addressed on 1Mbyte boundaries and only uses A20-A23. The 256K board is on 256K boundaries and uses A18-A23 for selection.

4.1.3 Address Mode Selection

Jumper W11 selects whether the EXPANDORAM IV board responds to extended addressing or to bank selection. Bank selection is used by processors which do not support the extended address bits (A16-A23) and is enabled by writing a user number to port FF, which enables one of five 48K banks on the 256K board.

4.1.4 Mode Selection (EDC or Parity)

Several jumpers are required to place the board in a specific operating mode. Jumpers W2 and W4 switch the data lines for EDC and parity. W6 selects the interrupt source; W9 and W13 enable the parity generators; and W18 and W19 select the source for write enables. The 8207 is programmed for the correct mode by the program word jumpers W7 and W10.

4.1.5 Interrupt Selection

Interrupts are selected by two jumpers. W6 selects the source for the interrupt, either parity or EDC, while W14 jumpers the interrupt to the IEEE-696 bus. Use of the interrupts is optional and at the discretion of the user.

4.1.6 Miscellaneous Options

Several other options are available on the EXPANDORAM IV board. Jumper W20 is the refresh option and selects between failsafe refresh only or failsafe and post OP CODE refresh. Jumper W15 selects on-board clock or bus clock. W8 selects whether the board will correct errors in EDC mode and W17 is the bank select input to the 8207. These options should usually be left in the factory installed positions, because there can be unexpected results if they are randomly changed.

4.2 PROGRAM DATA WORDS

After reset, the 8207 serially shifts in a program data word which is contained in jumpers W7 and W10. The standard configurations for parity and EDC are given in Table 4-1, and definitions for each bit are contained in the Jumper Definitions section of the Appendix called Jumpers and in the manufacturer's data sheets.

Table 4-1. JUMPER SETTINGS
(256K, extended address, 4 mHz CPU)

	Parity	EDC
W1	OUT	OUT
W2	IN LOWER POSITIONS (1-2, 4-5...22-23)	IN UPPER POSITIONS (2-3, 5-6...23-24)
W3	OUT	OUT
W4	IN LOWER POSITIONS	IN UPPER POSITIONS
W6	1-2	2-3

Table 4-1. JUMPER SETTINGS--Continued
(256K, extended address, 4 mHz CPU)

	Parity	EDC
W7	IN (1, 6, 8)	IN (2, 4, 5, 8)
W8	OUT	2-3
W9	IN	OUT
W10	IN (1, 3, 4, 6, 7, 8)	IN (1, 2, 5, 7)
W11	OUT	OUT
W12	IN (1, 2, 3, 4, 7, 8)	IN (1, 2, 3, 4, 7, 8)
W13	IN	OUT
W14	1-20 (VI0)	1-20
W15	1-2	1-2
W17	4-5	4-5
W18	2-3	1-2
W19	1-2	2-3
W20	2-3	2-3
W21	OUT	OUT
W22	1-2	1-2
W23	2-3	2-3

4.3 MEMORY UTILIZATION (Bank Select Mode)

When the bank select option is chosen (W11 in), the EXPANDORAM IV board emulates the operation of the SDSystems EXPANDORAM III board. This mode uses a PROM to produce the memory partitions required by specific operating systems and a user writable latch to specify the user number.

4.3.1 PROM

The PROM shipped with the EXPANDORAM IV board is designed for either operating systems which utilize a 48K or 56K memory partition per page. A page of memory is typically reserved for each user in an operating system allocation. The page number is equivalent to a user number. In the EXPANDORAM IV PROM, users (pages) 0-F are set as 48K pages with a 16K common area, and users 10-1F are set as 56K pages with an 8K common area.

The PROM has 9 address lines (A0-A8) which are divided into 2 fields: (U) user number (A4-A8) and (B) bank number (A0-A3). The U field is created by the 5 bit latch at port FF. The system writes the

user number to this port, and the PROM takes the number along with the high order system address lines (A12-A15) to access the data. The data output is the RAM address lines (A12-A19).

4.3.2 Switch Settings

Switch settings information on SW1 for the EXPANDORAM IV is given in Table 4-2. In the bank select mode, port FF is used to select the 48K memory page for access. The pages are accessed by outputting the page number to port FF. See Table 4-3 for page mapping and PROM program information. See also the Appendix called PROM Bank Select Program for additional information.

Table 4-2. MEMORY ADDRESS AND SIZE JUMPERS

EXTENDED ADDRESSING

256K W12-1, W12-2, W12-3, W12-4, W12-7, W12-8
1M W12-1, W12-2, W12-3, W12-4

Address Range 256K Memory	Switch SW1 1	2	3	4	5	6	7	8
000000-03FFFF	ON	ON	ON	ON	ON	ON	OFF	OFF
040000-07FFFF	ON	ON	ON	ON	ON	OFF	OFF	OFF
080000-0BFFFF	ON	ON	ON	ON	OFF	ON	OFF	OFF
0C0000-0FFFFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF
100000-13FFFF	ON	ON	ON	OFF	ON	ON	OFF	OFF
140000-17FFFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF
180000-1BFFFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF
1C0000-1FFFFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
200000-23FFFF	ON	ON	OFF	ON	ON	ON	OFF	OFF
240000-27FFFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF
280000-2BFFFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF
2C0000-2FFFFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
300000-33FFFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
340000-37FFFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF
380000-3BFFFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF
3C0000-3FFFFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
400000-43FFFF	ON	OFF	ON	ON	ON	ON	OFF	OFF
440000-47FFFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF
480000-4BFFFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF
4C0000-4FFFFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF
500000-53FFFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF
540000-57FFFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF
580000-5BFFFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF
5C0000-5FFFFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF
600000-63FFFF	ON	OFF	OFF	ON	ON	ON	OFF	OFF
640000-67FFFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF
680000-6BFFFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF
6C0000-6FFFFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
700000-73FFFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
740000-77FFFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
780000-7BFFFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
7C0000-7FFFFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
800000-83FFFF	OFF	ON	ON	ON	ON	ON	OFF	OFF
840000-87FFFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF
880000-8B0000	OFF	ON	ON	ON	OFF	ON	OFF	OFF

Table 4-2. MEMORY ADDRESS AND SIZE JUMPERS--Continued

Address Range 256K Memory	Switch SW1 1	2	3	4	5	6	7	8
8C0000-8FFFFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
900000-93FFFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF
940000-97FFFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF
980000-9BFFFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF
9C0000-9FFFFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
A00000-A3FFFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF
A40000-A7FFFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF
A80000-ABFFFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF
AC0000-AFFFFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
B00000-B3FFFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
B40000-B7FFFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF
B80000-BBFFFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
BC0000-BFFFFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
C00000-C3FFFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF
C40000-C7FFFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
C80000-CBFFFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF
CC0000-CFFFFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
D00000-D3FFFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
D40000-D7FFFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF
D80000-DBFFFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
DC0000-DFFFFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
E00000-E3FFFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
E40000-E7FFFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
E80000-EBFFFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
EC0000-EFFFFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
F00000-F3FFFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
F40000-F7FFFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
F80000-FBFFFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
FC0000-FFFFFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Address Range 1M Memory	Switch SW1 1	2	3	4	5	6	7	8
000000-0FFFFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF
100000-1FFFFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
200000-2FFFFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
300000-3FFFFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
400000-4FFFFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF
500000-5FFFFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF

Table 4-2. MEMORY ADDRESS AND SIZE JUMPERS--Continued

Address Range 1M Memory	Switch SW1 1	2	3	4	5	6	7	8
600000-6FFFFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
700000-7FFFFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
800000-8FFFFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
900000-9FFFFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
A00000-AFFFFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
B00000-BFFFFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
C00000-CFFFFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
D00000-DFFFFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
E00000-EFFFFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
F00000-FFFFFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

BANK SELECT MODE ADDRESSING

NOTE: Different switch settings are given so that more than one EXPANDORAM IV board can be used in a system.

256K W12-7, W12-8
1M All jumpers are out on W12

Board Number 256K Memory	Switch SW1 1	2	3	4	5	6	7	8
1	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
2	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
3	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

1Mbyte Memory	Switch SW1 1	2	3	4	5	6	7	8
1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Table 4-3. PROM PROGRAM AND PAGE MAPPING

(X=not defined; U=user number)

Users 0-F (16K Common)

16K Bank #	64K Pages (0-F)															
	256K				256K				256K				256K			
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3	Common	4	4	4	F	9	9	9	F	E	E	E	F	X	X	X
2	U=0	1	2	3	5	6	7	8	A	B	C	D	X	X	X	X
1	U=0	1	2	3	5	6	7	8	A	B	C	D	X	X	X	X
0	U=0	1	2	3	5	6	7	8	A	B	C	D	X	X	X	X

Users 10-1F (8K Common)

8K Bank #	64K Pages (0-F)															
	256K				256K				256K				256K			
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
7	Common	18	18	18	18	18	18	18	1F	1F	1F	1F	1F	1F	1F	X
6	U=10	11	12	13	14	15	16	17	19	1A	1B	1C	1D	1E	X	X
5	U=10	11	12	13	14	15	16	17	19	1A	1B	1C	1D	1E	X	X
4	U=10	11	12	13	14	15	16	17	19	1A	1B	1C	1D	1E	X	X
3	U=10	11	12	13	14	15	16	17	19	1A	1B	1C	1D	1E	X	X
2	U=10	11	12	13	14	15	16	17	19	1A	1B	1C	1D	1E	X	X
1	U=10	11	12	13	14	15	16	17	19	1A	1B	1C	1D	1E	X	X
0	U=10	11	12	13	14	15	16	17	19	1A	1B	1C	1D	1E	X	X

4.4 TEST PROCEDURE

The preliminary method for testing the EXPANDORAM IV will consist of an SBC-300 and an EXPANDORAM IV. The preliminary software will reside in the monitor ROM. The procedure for implementing this test is discussed below.

1. First be sure you have an SBC-300 with proper firmware. (V1.2 Monitor or later.)

2. Insert the SBC-300 into the system.

3. Set the board to address 040000H and to the proper mode (see Table 4-1).

4. Insert the EXPANDORAM IV into the system.

5. Run the SBC-300 extended memory test for addresses 400-7FF. (.J 400 7FF <cr>.)

6. The test will respond with a "P" if it passes and an error message if it fails.

SECTION V
ENVIRONMENTAL CONSIDERATIONS

5.0 GENERAL

The maximum recommended ambient operating temperature is 50°C (122°F).

5.1 POWER REQUIREMENTS

	8V
EDC	1.6A
Parity	1.3A

5.2 PHYSICAL SPECIFICATIONS

The EXPANDORAM IV is contained on a multi-layer printed circuit board which conforms to the IEEE-696 specification. The board dimensions are 5.125″ x 10.0″. No components extend more than 0.50″ from the component side of the board or more than 0.125″ from the solder side of the board.

APPENDIX A
SELECTED IEEE-696 SPECIFICATION SHEETS

NOTE: For additional information, see the complete document "IEEE Standard 696 Interface Devices."

IEEE-696 bus pin list

Pin No.	Signal & Type	Active Level	Description
1	+8 V(B)		Instantaneous minimum greater than 7 V, instantaneous maximum less than 25 V, average maximum less than 11 V.
2	+16 V(B)		Instantaneous minimum greater than 14.5 V, instantaneous maximum less than 35 V, average maximum less than 21.5 V.
3	XRDY (S)	H	One of two ready inputs to the current bus master. The bus is ready when both these ready inputs are true. See pin 72.
4	VI0*(S)	L OC	Vectored interrupt line 0.
5	VI1*(S)	L OC	Vectored interrupt line 1.
6	VI2*(S)	L OC	Vectored interrupt line 2.
7	VI3*(S)	L OC	Vectored interrupt line 3.
8	VI4*(S)	L OC	Vectored interrupt line 4.
9	VI5*(S)	L OC	Vectored interrupt line 5.
10	VI6*(S)	L OC	Vectored interrupt line 6.
11	VI7*(S)	L OC	Vectored interrupt line 7.
12	NMI*(S)	L OC	Non-maskable interrupt.

Pin No.	Signal & Type	Active Level	Description
13	PWRFAIL*(B)	L	Power fail bus signal.
14	TMA3* (M)	L OC	Temporary master priority bit 3.
15	A18 (M)	H	Extended address bit 18.
16	A16 (M)	H	Extended address bit 16.
17	A17 (M)	H	Extended address bit 17.
18	SDSB* (M)	L OC	The signal to disable the 8 status signals.
19	CDSB* (M)	L OC	The signal to disable the 5 control output signals.
20	O V(B)		Common with pin 100.
21	NDEF		Not to be defined. Manufacturer must specify any use in detail.
22	ADSB* (M)	L OC	The signal to disable the address signals.
23	DODSB* (M)	L OC	The control signal to disable the data output signals. (D07-0 for 8 bit transfers, ED7-0 and 0D7-0 for 16 bit transfers.
24	ϕ (B)	A	The master timing signal for the bus.
25	pSTVAL*(M)	L	Status valid strobe.
26	pHLDA(M)	H	A control signal used in conjunction with HOLD* to coordinate bus master transfer operations.
27	RFU		Reserved for future use.

Pin No.	Signal & Type	Active Level	Description
28	RFU		Reserved for future use.
29	A5 (M)	H	Address bit 5.
30	A4 (M)	H	Address bit 4.
31	A3 (M)	H	Address bit 3.
32	A15 (M)	H	Address bit 15 (most significant for non-extended addressing).
33	A12 (M)	H	Address bit 12.
34	A9 (M)	H	Address bit 9.
35	DO1 (M)/ED1 (M/S)	H	Data out bit 1, bidirectional even data bit 1.
36	DO0 (M)/ED0 (M/S)	H	Data out bit 0, bidirectional even data bit 0.
37	A10 (M)	H	Address bit 10.
38	DO4 (M)/ED4 (M/S)	H	Data out bit 4, bidirectional even data bit 4.
39	DO5 (M)/ED5 (M/S)	H	Data out bit 5, bidirectional even data bit 5.
40	DO6 (M)/ED6 (M/S)	H	Data out bit 6, bidirectional even data bit 6.
41	DI2 (S)/OD2 (M/S)	H	Data in bit 2, bidirectional odd data bit 2.
42	DI3 (S)/OD3 (M/S)	H	Data in bit 3, bidirectional odd data bit 3.
43	DI7 (S)/OD7 (M/S)	H	Data in bit 7, bidirectional odd data bit 7.

Pin No.	Signal & Type	Active Level	Description
44	sM1 (M)	H	The status signal which indicates that the current cycle is an op-code fetch.
45	sOUT (M)	H	The status signal identifying the data transfer bus cycle to an output device.
46	sINP (M)	H	The status signal identifying the data transfer bus cycle from an input device.
47	sMEMR (M)	H	The status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycle(s).
48	sHLTA (M)	H	The status signal which acknowledges that a HLT instruction has been executed.
49	CLOCK(B)	A	2 MHz (+0.5%) 40-60% duty cycle. Not required to be synchronous with any other bus signal.
50	O V (B)		Common with pin 100.
51	+8 V(B)		Common with pin 1.
52	-16 V(B)		Instantaneous maximum less than -14.5 V, instantaneous minimum greater than -35 V, average minimum greater than -21.5 V.
53	O V(B)		Common with pin 100.

Pin No.	Signal & Type	Active Level	Description
54	SLAVE CLR* (B)	L OC	A reset signal to reset bus slaves. Must be active with POC* and may also be generated by external means.
55	TMA0* (M)	L OC	Temporary master priority bit 0.
56	TMA1* (M)	L OC	Temporary master priority bit 1.
57	DMA2* (M)	L OC	Temporary master priority bit 2.
58	sXTRQ* (M)	L	The status signal which requests 16-bit slaves to assert SIXTN*.
59	A19 (M)	H	Extended address bit 19.
60	SIXTN* (S)	L OC	The signal generated by 16-bit slaves in response to the 16 bit request signal sXTRQ*.
61	A20 (M)	H	Extended address bit 20.
62	A21 (M)	H	Extended address bit 21.
63	A22 (M)	H	Extended address bit 22.
64	A23 (M)	H	Extended address bit 23.
65	NDEF		Not to be defined signal.
66	NDEF		Not to be defined signal.
67	PHANTOM* (M/S)	L OC	A bus signal which disables normal slave devices and enables phantom slaves--primarily used for bootstrapping systems without hardware front panels.
68	MWRT (B)	H	pWR*-sOUT (logic equation). This signal must follow pWR* by not more than 30 ns.

Pin No.	Signal & Type	Active Level	Description
69	RFU		Reserved for future use.
70	O V(B)		Common with pin 100.
71	RFU		Reserved for future use.
72	RDY (S)	H OC	See comments for pin 3.
73	INT* (S)	L OC	The primary interrupt request bus signal.
74	HOLD* (S)	L OC	The control signal used in conjunction with pHLDA to coordinate bus master transfer operations.
75	RESET* (B)	L OC	The reset signal to reset bus master devices. This signal must be active with POC* and may also be generated by external means.
76	pSYNC (M)	H	The control signal identifying BS_1.
77	pWR* (M)	L	The control signal signifying the presence of valid data on DO bus or data bus.
78	pDBIN (M)	H	The control signal that requests data on the DI bus or data bus from the currently addressed slave.
79	A0 (M)	H	Address bit 0 (least significant).
80	A1 (M)	H	Address bit 1.
81	A2 (M)	H	Address bit 2.
82	A6 (M)	H	Address bit 6.

Pin No.	Signal & Type	Active Level	Description
83	A7 (M)	H	Address bit 7.
84	A8 (M)	H	Address bit 8.
85	A13(M)	H	Address bit 13.
86	A14(M)	H	Address bit 14.
87	A11(M)	H	Address bit 11.
88	DO2 (M)/ED2 (M/S)	H	Data out bit 2, bidirectional even data bit 2.
89	DO3 (M)/ED3 (M/S)	H	Data out bit 3, bidirectional even data bit 3.
90	DO7 (M)/ED7 (M/S)	H	Data out bit 7, bidirectional even data bit 7.
91	DI4 (S)/OD4 (M/S)	H	Data in bit 4 and bidirectional odd data bit 4.
92	DI5 (S)/OD5 (M/S)	H	Data in bit 5 and bidirectional odd data bit 5.
93	DI6 (S)/OD6 (M/S)	H	Data in bit 6 and bidirectional odd data bit 6.
94	DI1 (S)/OD1 (M/S)	H	Data in bit 1 and bidirectional odd data bit 1.
95	DI0 (S)/OD0 (M/S)	H	Data in bit 0 (least significant for 8 bit data) and bidirectional odd data bit 0.
96	sINTA (M)	H	The status signal identifying the bus input cycle(s) that may follow an accepted interrupt request presented on INT*.
97	sWO* (M)	L	The status signal identifying a bus cycle which transfers data from a bus master to a slave.

Pin No.	Signal & Type	Active Level	Description
98	ERROR* (S)	L OC	The bus status signal signifying an error condition during present bus cycle.
99	POC* (B)	L	The power-on clear signal for all bus devices; when this signal goes low, it must stay low for at least 10 millisecs.
100	O V(B)		System ground.

IEEE-696 BUS LAYOUT --- QUICK REFERENCE

pin 1	+8 V(B)	
pin 2	+16 V(B)	
pin 3	XRDY (S)	H
pin 4	VI0* (S)	L
pin 5	VI1* (S)	L
pin 6	VI2* (S)	L
pin 7	VI3* (S)	L
pin 8	VI4* (S)	L
pin 9	VI5* (S)	L
pin 10	VI6* (S)	L
pin 11	VI7* (S)	L
pin 12	NMI* (S)	L
pin 13	PWRFAIL*(B)	L
pin 14	TMA3*(M)	L
pin 15	A18(M)	H
pin 16	A16(M)	H
pin 17	A17(M)	H
pin 18	SDSB*(M)	L
pin 19	CDSB*(M)	L
pin 20	O V	
pin 21	NDEF	
pin 22	ADSB*(M)	L
pin 23	DODSB*(M)	L
pin 24	ϕ(B)	A
pin 25	pSTVAL*(M)	L
pin 26	pHLDA (M)	H
pin 27	RFU	
pin 28	RFU	
pin 29	A5(M)	H
pin 30	A4(M)	H
pin 31	A3(M)	H
pin 32	A15(M)	H
pin 33	A12(M)	H
pin 34	A9(M)	H
pin 35	DO1(M)/ED1 (M/S)	H
pin 36	DOO(M)/EDO(M/S)	H
pin 37	A10(M)	H
pin 38	DO4(M)/ED4(M/S)	H
pin 39	DO5(M)/ED5(M/S)	H
pin 40	DO6(M)/ED6(M/S)	H
pin 41	DI2(S)/OD2(M/S)	H
pin 42	DI3(S)/OD3(M/S)	H
pin 43	DI7(S)/OD7(M/S)	H
pin 44	sM1(M)	H
pin 45	sOUT(M)	H
pin 46	sINP	H
pin 47	sMEMR	H
pin 48	sHLTA(M)	H
pin 49	CLOCK(B)	A
pin 50	OV	
pin 51	+8 V(B)	
pin 52	-16 V(B)	
pin 53	O V	
pin 54	SLAVE CLR* (B)	L
pin 55	TMAO*(M)	L
pin 56	TMA1*(M)	L
pin 57	TMA2*(M)	L
pin 58	sXTRQ*(M)	L
pin 59	A19(M)	H
pin 60	SIXTN*(S)	L
pin 61	A20(M)	H
pin 62	A21(M)	H
pin 63	A22(M)	H
pin 64	A23(M)	H
pin 65	NDEF	
pin 66	NDEF	
pin 67	PHANTOM*(M/S)	L
pin 68	MWRT (B)	H
pin 69	RFU	
pin 70	O V	
pin 71	RFU	
pin 72	RDY (S)	H
pin 73	INT*(S)	L
pin 74	HOLD*(M)	L
pin 75	RESET* (B)	L
pin 76	pSYNC(M)	H
pin 77	pWR*(M)	L
pin 78	pDBIN(M)	H
pin 79	AO (M)	H
pin 80	A1(M)	H
pin 81	A2(M)	H
pin 82	A6(M)	H
pin 83	A7(M)	H
pin 84	A8(M)	H
pin 85	A13(M)	H
pin 86	A14(M)	H
pin 87	A11(M)	H
pin 88	DO2(M)/ED2(M/S)	H
pin 89	DO3(M)/ED3(M/S)	H
pin 90	DO7(M)/ED7(M/S)	H
pin 91	DI4(S)/OD4(M/S)	H
pin 92	DI5(S)/OD5(M/S)	H
pin 93	DI6(S)/OD6(M/S)	H
pin 94	DI1(S)/OD1(M/S)	H
pin 95	DI0(S)/ODO(M/S)	H
pin 96	sINTA(M)	H
pin 97	sWO*(M)	L
pin 98	ERROR*(S)	L
pin 99	POC*(B)	
pin 100	O V	

APPENDIX B
DISCLAIMER

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APPENDIX C
LIMITED WARRANTY

All SDSystems printed circuit board assemblies are warranted for a period of one (1) year from date of invoice to be free from defects of material and workmanship.

Should an SDSystems board fail to perform to specifications, obtain a Return Material Authorization (RMA) number from your distributor or from SDSystems. Include this number in all correspondence and with the returned product. Ship the item prepaid to SDSystems and it will, at our option, be repaired or replaced free of charge provided the unit is received during the warranty period.

In order to validate this warranty, the enclosed warranty card must be returned to SDSystems. If no warranty card is on file at the time of product return, dated proof of purchase will be required.

This warranty is invalid if product has been misused or improperly modified. Modifications documented in the SDSystems unit publications may be performed without invalidating the warranty. All other modifications will invalidate the warranty. Warranty is limited to replacement of defective parts and no responsibility is assumed for damage to other equipment.

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APPENDIX D
PERFORMANCE SPECIFICATIONS

TOPIC	DATA	
Interface Levels	TTL Compatible	
Memory Capacity	256K bytes to 1Mbyte	
Memory Device Access	200 ns	
	PARITY	EDC
Memory Board Access	400 ns	750 ns

APPENDIX E
JUMPERS

A. MEMORY SIZE - EXTENDED ADDRESSING

Jumper	256K Bytes	1Mbyte
W12-1, 2, 3, 4	IN	IN
W12-5, 6	OUT	OUT
W12-7, 8	IN	OUT
W1-1	OUT	IN
W3-1	OUT	IN
W11-1	OUT	OUT

B. MEMORY SIZE - BANK SELECT MODE ADDRESSING

Jumper	256K Bytes	1Mbyte
W12-1, 2, 3, 4, 5, 6	OUT	OUT
W12-7, 8	IN	OUT
W1-1	OUT	IN
W3-1	OUT	IN
W11-1	IN	IN

C. HOST CPU OPTIONS

	Jumper	IEEE-696	SBC-200
sWO*	W22	1-2	2-3
sXTRQ*	W21	OUT	IN

D. MEMORY MODE

Chip/Jumper	ECC	Parity
U13	IN	OUT
U35, 36, 46, 47, 57, 58, 68, 69	IN	OUT
W9, W13	OUT	IN
W18	1-2	2-3

D. MEMORY MODE--Continued

	Chip/Jumper	ECC	Parity
	W19	2-3	1-2
	W6	2-3	1-2
Data Buses	W2	2-3, 5-6, 8-9, 11-12, 14-15, 17-18, 20-21, 23-24	1-2, 4-5, 7-8, 10-11, 13-14, 16-17, 19-20, 22-23
Data Buses	W4	2-3, 5-6, 8-9, 11-12, 14-15, 17-18, 20-21, 23-24	1-2, 4-5, 7-8, 10-11, 13-14, 16-17, 19-20, 22-23

E. 8207 PROGRAM DATA WORD (For 16 mHz Clock)

8207 Jumpers		ECC			Parity		
			Clock Speed			Clock Speed	
Program Data Bit	Jumper	8207 Signal	16 mHz	5/8 mHz	8207 Signal	16 mHz	5/8 mHz
PD0	W7-6	ECC	OUT	OUT	ECC	IN	IN
PD1	W7-4	SA	IN	IN	SA*	OUT	OUT
PD2	W7-3	SB*	OUT	OUT	SB	OUT	OUT
PD3	W7-1	CFS	OUT	IN	CFS*	IN	OUT
PD4	W7-2	RFS	IN	IN	RFS*	OUT	OUT
PD5	W7-8	XA*	IN	IN	RB0*	IN	IN
PD6	W7-7	XB	OUT	OUT	RB1*	OUT	OUT
PD7	W7-5	CI1*	IN	IN	CI1	OUT	OUT
PD8	W10-5	CI2*	IN	IN	CI2	OUT	OUT
PD9	W10-4	PLS	OUT	OUT	PLS*	IN	IN
PD10	W10-3	EXT*	OUT	OUT	EXT	IN	IN
PD11	W10-1	FFS	OUT	IN	FFS*	IN	OUT
PD12	W10-2	PPR	IN	IN	PPR*	OUT	OUT
PD13	W10-6	RB0	OUT	OUT	TM1	IN	IN
PD14	W10-7	RB1	IN	IN	0	IN	IN
PD15	W10-8	TM2*	OUT	OUT	0	IN	IN

F. NON-ECC MODE PROGRAM DATA WORD

Program Data Bit	Name	Polarity/Function	Berg Jumper
PD0	ECC	ECC=0 FOR NON-ECC MODE	W7-6
PD1	SA*	SA*=0 PORT A IS SYNCHRONOUS	W7-4
		SA*=1 PORT A IS ASYNCHRONOUS	
PD2	SB	SB=0 PORT B IS ASYNCHRONOUS	W7-3
		SB=1 PORT B IS SYNCHRONOUS	
PD3	CFS*	CFS*=0 FAST-CYCLE iAPX 286 MODE	W7-1
		CFS*=1 SLOW-CYCLE iAPX 86 MODE	
PD4	RFS*	RFS*=0 FAST RAM	W7-2
		RFS*=1 SLOW RAM	
PD5	RB0*	RAM BANK OCCUPANCY BIT 0	W7-8
PD6	RB1*	RAM BANK OCCUPANCY BIT 1	W7-7
PD7	CI1	COUNT INTERVAL BIT 1	W7-5
PD8	CI0	COUNT INTERVAL BIT 0	W10-5
PD9	PLS*	PLS*=0 LONG REFRESH PERIOD	W10-4
		PLS*=1 SHORT REFRESH PERIOD	
PD10	EXT	EXT=0 NOT EXTENDED	W10-3
		EXT=1 EXTENDED	
PD11	FFS*	FFS*=0 FAST CPU FREQUENCY	W10-1
		FFS*=1 SLOW CPU FREQUENCY	
PD12	PPR*	PPR*=0 MOST RECENTLY USED PORT PRIORITY	W10-2
		PPR*=1 PORT A PREFERRED PRIORITY	
PD13	TM1	TM1=0 TEST MODE 1 OFF	W10-6
		TM1=1 TEST MODE 1 ENABLED	
PD14	0	RESERVED MUST BE ZERO	W10-7
PD15	0	RESERVED MUST BE ZERO	W10-8

G. ECC MODE PROGRAM DATA WORD

Program Data Bit	Name	Polarity/Function		Berg Jumper
PD0	ECC	ECC=1	ECC MODE	W7-6
PD1	SA	SA=0	PORT A IS ASYNCHRONOUS	W7-4
		SA=1	PORT A IS SYNCHRONOUS	
PD2	SB*	SB*=0	PORT B IS SYNCHRONOUS	W7-3
		SB*=1	PORT B IS ASYNCHRONOUS	
PD3	CFS	CFS=0	SLOW-CYCLE iAPX 86 MODE	W7-1
		CFS=1	FAST-CYCLE iAPX 286 MODE	
PD4	RFS	RFS=0	SLOW RAM	W7-2
		RFS=1	FAST RAM	
PD5	XA*	XA*=0	MULTIBUS-COMPATIBLE ACKA	W7-8
		XA*=1	ADVANCED ACKA NOT MULTIBUS COMPATIBLE	
PD6	XB	XB=0	ADVANCED ACKB NOT MULTIBUS COMPATIBLE	W7-7
		XB=1	MULTIBUS-COMPATIBLE ACKB	
PD7	CI1*	COUNT INTERVAL BIT 1		W7-5
PD8	CI0*	COUNT INTERVAL BIT 0		W10-5
PD9	PLS	PLS=0	SHORT REFRESH PERIOD	W10-4
		PLS=1	LONG REFRESH PERIOD	
PD10	EXT*	EXT*=0	MASTER AND SLAVE EDCU	W10-3
		EXT*=1	MASTER EDCU ONLY	
PD11	FFS	FFS=0	SLOW CPU FREQUENCY	W10-1
		FFS=1	FAST CPU FREQUENCY	
PD12	PPR	PPR=0	PORT A PREFERRED PRIORITY	W10-2
		PPR=1	MOST RECENTLY USED PORT PRIORITY	
PD13	RB0	RAM BANK OCCUPANCY BIT 0		W10-6
PD14	RB1	RAM BANK OCCUPANCY BIT 1		W10-7
PD15	TM2*	TM2*=0	TEST MODE 2 ENABLED	W10-8
		TM2*=1	TEST MODE 2 OFF	

H. REFRESH

	Post OP CODE Refresh	Failsafe Refresh Only
W20	1-2	2-3

I. ERROR INTERRUPT (IEEE-696 Bus)

Jumper	Bus Line
W14-1	VI0*
-2	VI1*
-3	VI2*
-4	VI3*
-5	VI4*
-6	VI5*
-7	VI6*
-8	VI7*
-9	NMI*
-10	ERROR*

J. OPTION JUMPERS

CLOCK	ON-BOARD 16 mHz	W15-1, 2
	BUS CLOCK	W15-2, 3
CRCT	CORRECT ERRORS	W8-2, 3
	DON'T CORRECT	W8-1, 2
BS1	STANDARD RAS/CAS	W17-4, 5
PAL READ SELECT	pDBIN	W23-2, 3
	SMEMR	W23-1, 2
REFRESH	FAILSAFE ONLY	W20-2, 3
	POST OP CODE & FAILSAFE	W20-1, 2

K. JUMPER DEFINITIONS

Jumper	Definition		
W1	Even/low bank address bit A8 for 256K RAM capability		IN 256K RAMs OUT 64K/16K RAMs
W2	Data-out bus jumpers (switch data bus for EDC/non-EDC operation)		All down (1-2...) Parity All up (2-3...) EDC
W3	Odd/high bank address bit A8		IN 256K RAMs OUT 64K/16K RAMs
W4	Data-in bus jumpers		All down (1-2...) Parity All up (2-3...) EDC
W5	Not used		
W6	Interrupt source select		1-2 Parity error 2-3 EDC error
W7	Program word 1		
W8	Correct error jumper (EDC only) (CRCT pin input)		1-2 Don't correct errors 2-3 Correct errors
W9	Parity enable for even/low bank		IN Enabled OUT Disabled
W10	Program word 2		
W11	Extended address/bank select mode		IN Bank mode OUT Extended address
W12	Memory size select	256K	IN 1, 2, 3, 4, 7, 8 OUT 5, 6
		1Mbyte	IN 1, 2, 3, 4 OUT 5, 6, 7, 8
W13	Parity enable for odd/high bank		IN Enabled OUT Disabled

W14 Interrupt select	
1-20	VI0 (Vectored Interrupt 0)
2-19	VI1
3-18	VI2
4-17	VI3
5-16	VI4
6-15	VI5
7-14	VI6
8-13	VI7
9-12	NMI
10-11	ERROR

K. JUMPER DEFINITIONS--Continued

Jumper		Definition
W15	Clock select	1-2 On board 2-3 Bus clock
W16	Not used	
W17	Bank selection (BS1 input)	1-2 A17 to BS1 2-3 A19 to BS1 3-4 A19 to BS1 4-5 GND to BS1 (standard)
W18	Even/low bank write enable	1-2 EDC 2-3 Parity mode
W19	Odd/high bank write enable	1-2 Parity mode 2-3 EDC
W20	Refresh select	1-2 M1 refresh 2-3 Failsafe refresh only
W21	16 bit enable	IN Pull-up for non-IEEE-696 OUT Standard
W22	sWO* select	1-2 Use sWO* 2-3 Use inverted sMEMR (for SBC-200)
W23	Read select for PAL	1-2 Select sMEMR 2-3 Select pDBIN for RDCMD*

APPENDIX F
PAL20L10 SPECIFICATION

```
MEMR SWO SOUT SXTRQ /DBIN MRJ /BRDSEL A0 /DBM
    MWRT SINP GND /PHAN /ENMEM /WEODD /ODDLOC
    /WRCMD /RDCMD /OVEREN /DOBEN /DIBEN /EVENLOC
    /WEEVEN VCC

IF(VCC)RDCMD =BRDSEL*MEMR*DBIN*/PHAN*/MRJ
+BRDSEL*MEMR*/PHAN*MRJ

IF(VCC)WRCMD=BRDSEL*/SOUT*/SINP*SWO*MWRT*/PHAN

IF(VCC)ENMEM=BRDSEL*MEMR*/PHAN+BRDSEL*/SOUT*
    /SINP*SWO*/PHAN

IF(VCC)ODDLOC=RDCMD*A0*/EVENLOC+ODDLOC*RDCMD
    +RDCMD*SXTRQ

IF(VCC)EVENLOC =RDCMD*/A0*/ODDLOC+EVENLOC*
    RDCMD+RDCMD*SXTRQ

IF(VCC)OVEREN=RDCMD*/SXTRQ*/A0+WRCMD*/SXTRQ*A0

IF(VCC)DIBEN =WRCMD*SXTRQ+BRDSEL*DBIN*MEMR*
    /PHAN

IF(VCC)DOBEN =BRDSEL*DBIN*MEMR*/PHAN*SXTRQ+
    SOUT+WRCMD

IF(VCC)WEEVEN =/DBM*SWO*/SOUT*/SINP*SXTRQ+SWO*
    /SOUT*/SINP*/A0*/DBM

IF(VCC)WEODD =/DBM*SWO*/SOUT*/SINP*SXTRQ+SWO*/
    SOUT*/SINP*A0*/DBM
DESCRIPTION:
```

APPENDIX G
PROM BANK SELECT PROGRAM
MMI6349-1

User	A12-A15															
No.	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
1	10	11	12	13	14	15	16	17	18	19	1A	1B	0C	0D	0E	0F
2	20	21	22	23	24	25	26	27	28	29	2A	2B	0C	0D	0E	0F
3	30	31	32	33	34	35	36	37	38	39	3A	3B	0C	0D	0E	0F
4	1C	1D	1E	1F	2C	2D	2E	2F	3C	3D	3E	3F	0C	0D	0E	0F
5	40	41	42	43	44	45	46	47	48	49	4A	4B	0C	0D	0E	0F
6	50	51	53	53	54	55	56	57	58	59	5A	5B	0C	0D	0E	0F
7	60	61	62	63	64	65	66	67	68	69	6A	6B	0C	0D	0E	0F
8	70	71	72	73	74	75	76	77	78	79	7A	7B	0C	0D	0E	0F
9	5C	5D	5E	5F	6C	6D	6E	6F	7C	7D	7E	7F	0C	0D	0E	0F
A	80	81	82	83	84	85	86	87	88	89	8A	8B	0C	0D	0E	0F
B	90	91	92	93	94	95	96	97	98	99	9A	9B	0C	0D	0E	0F
C	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	0C	0D	0E	0F
D	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	0C	0D	0E	0F
E	9C	9D	9E	9F	AC	AD	AE	AF	BC	BD	BE	BF	0C	0D	0E	0F
F	4C	4D	4E	4F	8C	8D	8E	8F	C0	C1	C2	C3	0C	0D	0E	0F
10	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
11	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	0E	0F
12	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	0E	0F
13	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	0E	0F
14	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	0E	0F
15	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	0E	0F
16	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	0E	0F
17	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	0E	0F
18	1E	1F	2E	2F	3E	3F	4E	4F	5E	5F	6E	6F	7E	7F	0E	0F
19	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	0E	0F
1A	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	0E	0F
1B	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	0E	0F
1C	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	0E	0F
1D	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	0E	0F
1E	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	0E	0F
1F	8E	8F	9E	9F	AE	AF	BE	BF	CE	CF	DE	DF	E0	E1	0E	0F

APPENDIX H
PARTS LIST FOR EXPANDORAM IV

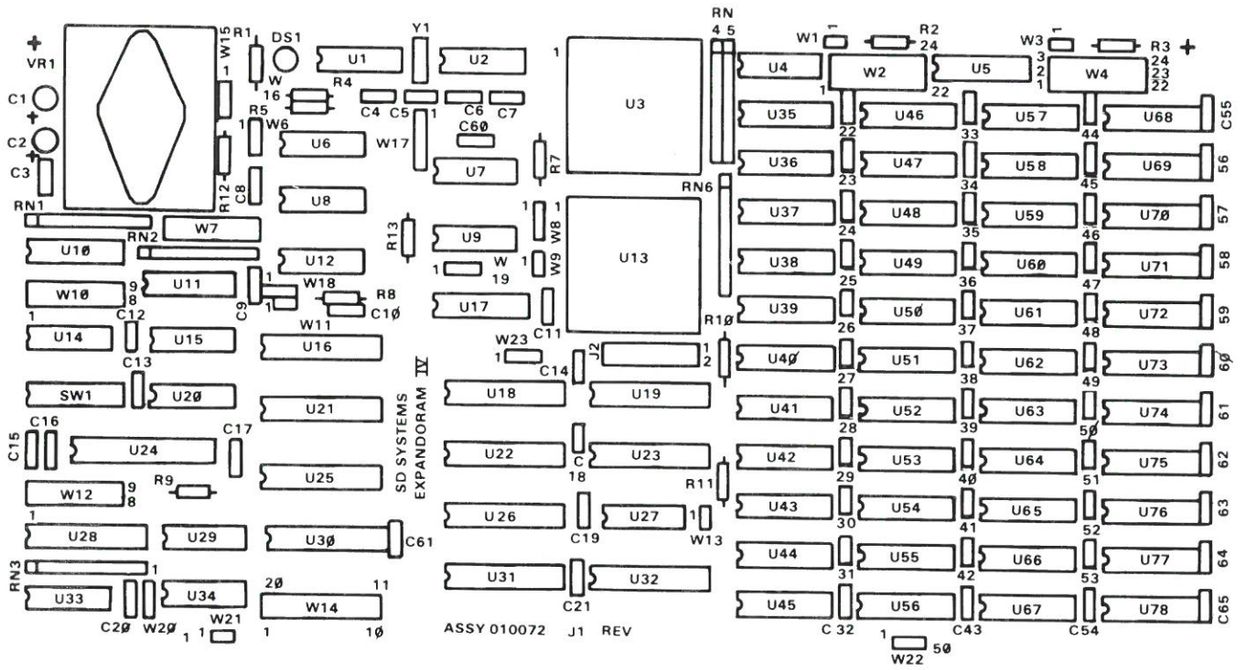
QTY REQD	DESCRIPTION	PART/SUB NUMBER	DESIGNATION
	EXPANDORAM IV		
0	BOARD SCHEMATIC, EXPANDORAM IV	0300721	
1	PC BOARD, EXPANDORAM IV	7000065	
1	IC, 7438	7010030	U6
1	IC, 74LS02	7010162	U20
2	IC, 74LS04	7010164	U2,U4
1	IC, 74LS08	7010166	U14
1	IC, 74LS10	7010168	U15
2	IC, 74LS14	7010172	U29, U34
1	IC, 74LS30	7010180	U7
1	IC, 74LS32	7010181	U12
4	IC, 74LS74	7010195	U1, U5, U8, U33
2	IC, 74LS165	7010235	U10, U11
1	IC, 74LS174	7010241	U17
6	IC, 74LS244	7010264	U21-U23, U25, U26, U30
2	IC, 74LS245	7010265	U31, U32
2	IC, 74LS280	7010279	U9, U27
2	IC, 74LS374	7010305	U18, U19
36	4164 RAM	7010422	U37-U45 U48-U56, U59-U67, U70-U78
3	4.7K OHM SIP	7010434	RN1-RN3
1	IC, 74LS682	7010518	U28
1	8207 8 MHZ	7010533	U3
3	SIP 10 PIN 220 OHM	7010525	RN4-RN6
4	RES 22 OHM 1/4W 5% CC	7020033	R10-R13
1	RES 220 OHM 1/4W 5% CC	7020057	R1
3	RES 1K OHM 1/4W 5% CC	7020073	R4, R5, R9
4	RES 4.7K OHM 1/4W 5%	7020089	R2, R3, R7, R8
1	CAP 150 PF	7030042	C6
1	CAP 300 PF 20% 50V .2	7030044	C5

QTY REQD	DESCRIPTION	PART/SUB NUMBER	DESIGNATION
	EXPANDORAM IV (Continued)		
1	.01 μF CAPACITOR	7030063	C4
62	.1 μF CAPACITOR	7030068	C3, C7-C67
2	CAP, 10 μF 35V TANT	7030080	C1, C2
1	DIP SWITCH, K40-D8	7050066	SW1
1	SOCKET, 68 PIN	7060027	XU3
1	16 MHZ CRYSTAL	7080021	Y1
1	HEATSINK TMH 6103-B	7130004	
1	78H05	7160012	VR1
6	BERG 1X2 STR .230 PIN TIN	7170018	W1, W3, W9, W11, W13, W21
8	BERG 1X3 STR .230 PIN TIN	7170021	W6, W8, W15, W18-W20, W22, W23
6	BERG STIK 2X8 TIN PL ST	7170100	W2, W4, W7, W10, W12, J2
1	BERG STIK ST 2X10 TIN PL	7170102	W14
2	BERG 1X8	7170103	W2, W4
1	BERG 1X5	7170104	W17
1	LED Z-80 STARTER	7180002	DS1
2	SCREW, PPH, 6-32 X 3/8	7130006	
2	NUT, HEX, 6-32	7130007	
2	LOCKWASHER, NO. 6	7130009	
2	EJECTOR, PCB	7130228	
42	65474 BERG PV JUMPER	7170004	
1	XRAM IV PROG. PROM	7250024	U24
1	XRAM IV PROG. PROM	7250018	U16
0	TEST PROC. ASSY. XRAM IV (PARITY)	0900722	
0	JUMPER TABLES	0600722	
	EXPANDORAM IV - EDC		
0	BOARD SCHEMATIC, EXPANDORAM IV	0300721	
1	PC BOARD, EXPANDORAM IV	7000065	
1	IC, 7438	7010030	U6
1	IC, 74LS02	7010162	U20

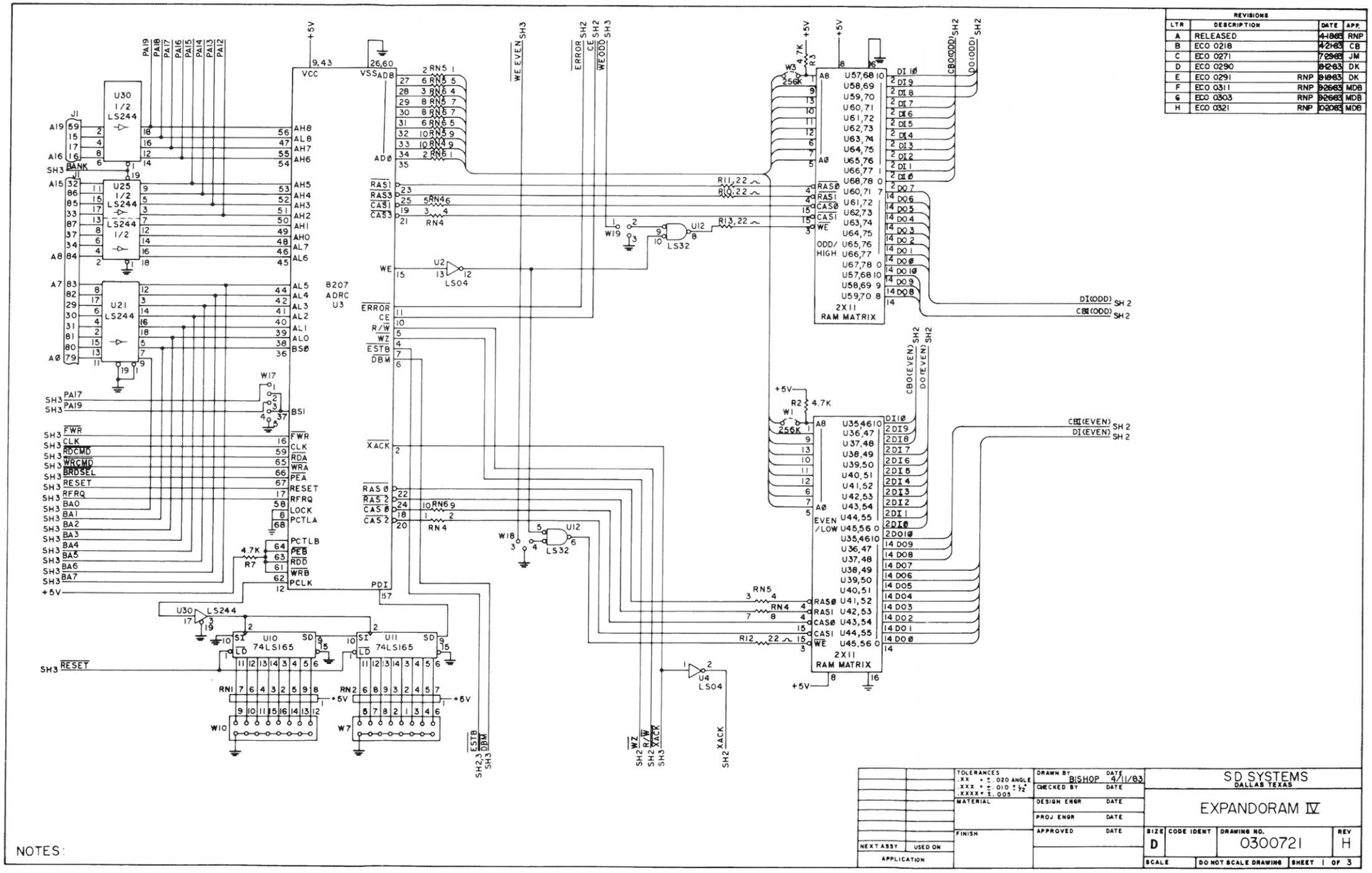
QTY REQD	DESCRIPTION	PART/SUB NUMBER	DESIGNATION
	EXPANDORAM IV - EDC (Continued)		
2	IC, 74LS04	7010164	U2, U4
1	IC, 74LS08	7010166	U14
1	IC, 74LS10	7010168	U15
2	IC, 74LS14	7010172	U29, U34
1	IC, 74LS30	7010180	U7
1	IC, 74LS32	7010181	U12
4	IC, 74LS74	7010195	U1, U5, U8, U33
2	IC, 74LS165	7010235	U10, U11
1	IC, 74LS174	7010241	U17
6	IC, 74LS244	7010264	U21-U23, U25, U26, U30
2	IC, 74LS245	7010265	U31, U32
2	IC, 74LS280	7010279	U9, U27
2	IC, 74LS374	7010305	U18, U19
44	4164 RAM	7010422	U35-U78
3	4.7K OHM SIP	7010434	RN1-RN3
1	IC, 74LS682	7010518	U28
1	IC, 8206 ERROR DET, CORR	7010521	U13
1	8207 8 MHZ	7010533	U3
3	SIP 10 PIN 220 OHM	7010525	RN4-RN6
4	RES 22 OHM 1/4W 5% CC	7020033	R10-R13
1	RES 220 OHM 1/4W 5% CC	7020057	R1
3	RES 1K OHM 1/4W 5% CC	7020073	R4, R5, R9
5	RES 4.7K OHM 1/4W 5%	7020089	R2, R3, R6-R8
1	CAP 150 PF	7030042	C6
1	CAP 300 PF 20% 50V .2	7030044	C5
1	.01 μF CAPACITOR	7030063	C4
62	.1 μF CAPACITOR	7030068	C3, C7-C67
2	CAP, 10 μF 35V TANT	7030080	C1, C2
1	DIP SWITCH, K40-D8	7050066	SW1
2	SOCKET, 68 PIN	7060027	XU3, XU13
1	8 MHZ CRYSTAL	7080007	Y1
1	HEATSINK TMH 6103-B	7130004	
1	78H05	7160012	VR1
6	BERG 1X2 STR .230 PIN TIN	7170018	W1, W3, W9, W11, W13, W21

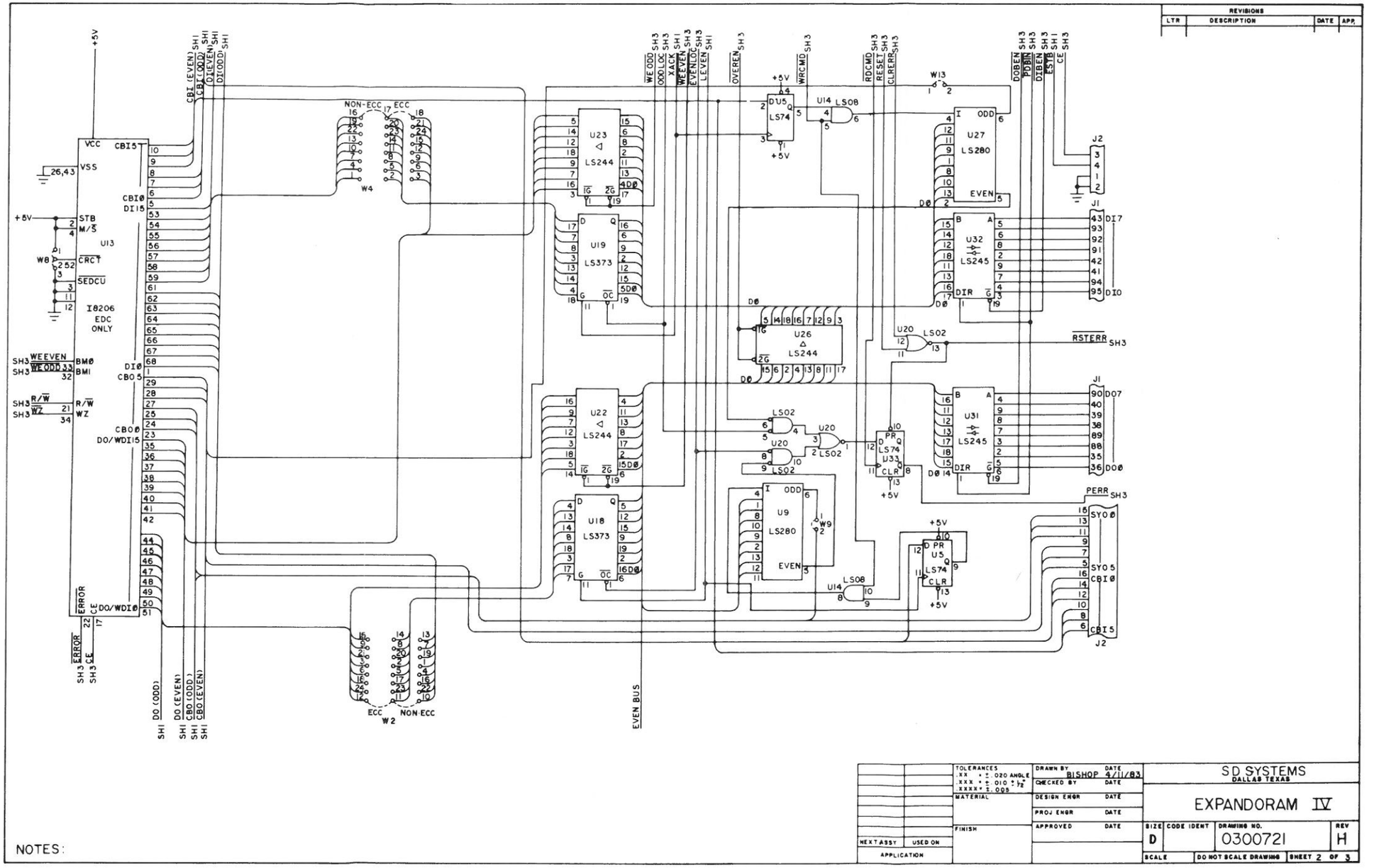
QTY REQD	DESCRIPTION	PART/SUB NUMBER	DESIGNATION
	EXPANDORAM IV - EDC (Continued)		
8	BERG 1X3 STR .230 PIN TIN	7170021	W6, W8, W15, W18-W20, W22, W23
6	BERG STIK 2X8 TIN PL ST	7170100	W2, W4, W7, W10, W12, J2
1	BERG STIK ST 2X10 TIN PL	7170102	W14
2	BERG 1X8	7170103	W2, W4
1	BERG 1X5	7170104	W17
1	LED Z-80 STARTER	7180002	DS1
2	SCREW, PPH, 6-32 X 3/8	7130006	
2	NUT, HEX, 6-32	7130007	
2	LOCKWASHER, NO. 6	7130009	
2	EJECTOR, PCB	7130228	
40	65474 BERG PV JUMPER	7170004	
1	XRAM IV PROG PROM	7250024	U24
1	XRAM IV PROG. PROM	7250018	U16
0	TEST PROC. ASSY. XRAM IV (EDC)	0900721	
0	JUMPER TABLES	0600721	

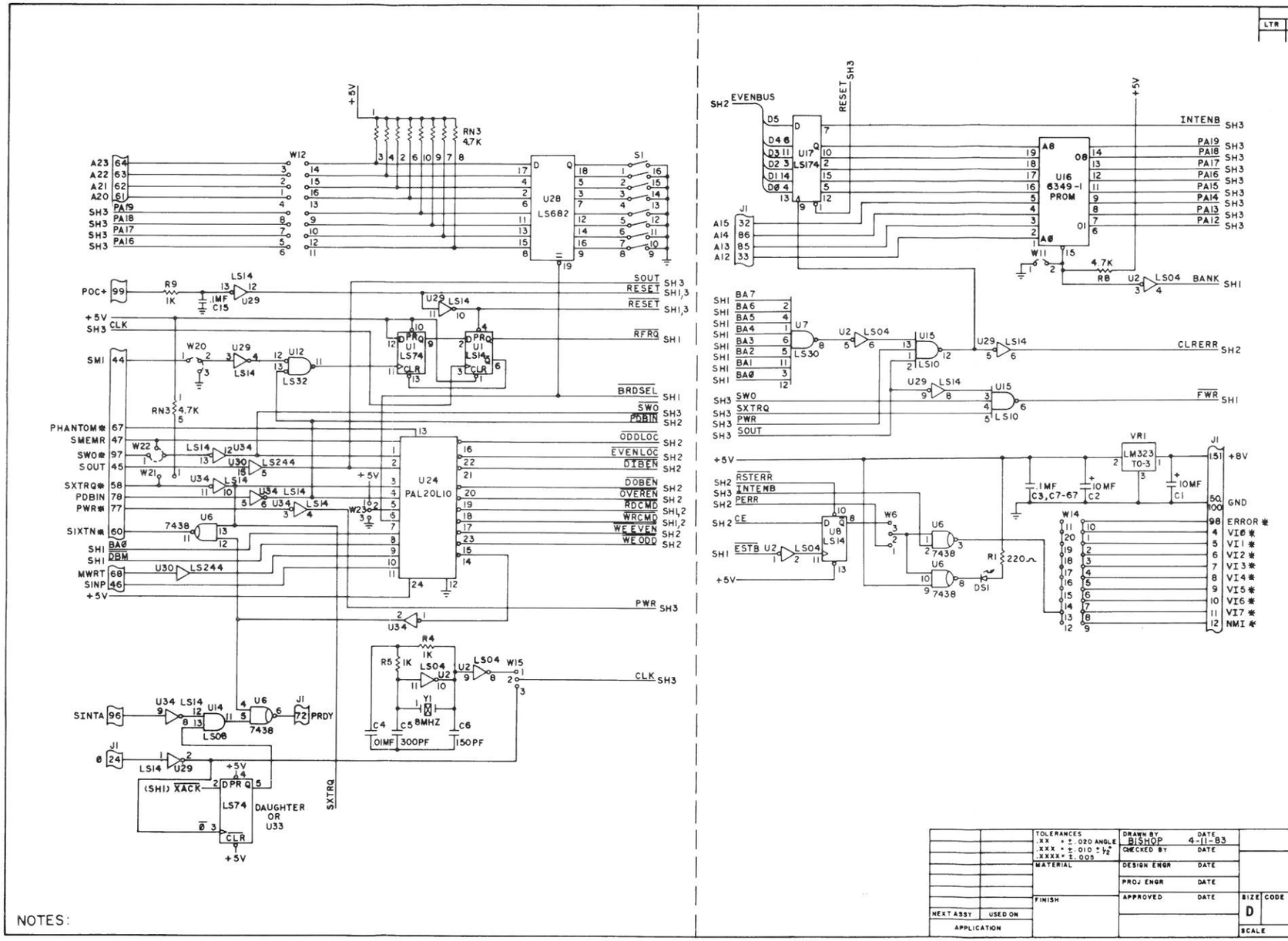
APPENDIX I
PARTS PLACEMENT DIAGRAM


SD SYSTEMS EXPANDORAM IV
ASSY 010072 J1 REV

APPENDIX J
SCHEMATIC


REVISIONS
LTR DESCRIPTION DATE APP.
A RELEASED 4-1883 RNP
B ECO 0218 4218? CB
C ECO 0271 7298? JM
D ECO 0290 8283 DK
E ECO 0291 RNP 91083 DK
F ECO 0311 RNP 92683 MDB
G ECO 0303 RNP 92683 MDB
H ECO 0321 RNP 02083 MDB
U30 1/2 LS244
U25 1/2 LS244
LS244 1/2
U21 LS244
8207 ADRC U3
U10 74LS165
U11 74LS165
U12 LS32
U2 LS04
U4 LS04
RAM MATRIX 2X11
NOTES:
SD SYSTEMS DALLAS TEXAS
EXPANDORAM IV
DRAWING NO. 0300721
REV H
SIZE D
SHEET 1 OF 3


REVISIONS
LTR DESCRIPTION DATE APP.
I8206 EDC ONLY
U13
U19 LS373
U18 LS373
U22 LS244
U23 LS244
U26 LS244
U27 LS280
U32 LS245
U31 LS245
U9 LS280
U5 LS74
U33 LS74
U14 LS08
U20 LS02
W2
W4
W8
W9
W13
J1
J2
NON-ECC
ECC
EVEN BUS
NOTES:
SD SYSTEMS
DALLAS TEXAS
EXPANDORAM IV
DRAWING NO. 0300721
REV H
SIZE D
SHEET 2 OF 3


REVISIONS
LTR DESCRIPTION DATE APP.
NOTES:
TOLERANCES .XX ± .020 ANGLE .XXX ± .010 ± ½° .XXXX ± .005
MATERIAL
FINISH
NEXT ASSY USED ON
APPLICATION
DRAWN BY BISHOP DATE 4-11-83
CHECKED BY DATE
DESIGN ENGR DATE
PROJ ENGR DATE
APPROVED DATE
SD SYSTEMS
DALLAS TEXAS
EXPANDORAM IV
SIZE D
CODE IDENT
DRAWING NO. 0300721
REV H
SCALE DO NOT SCALE DRAWING
SHEET 3 OF 3

APPENDIX K
JUMPER NUMBERING NOTATION

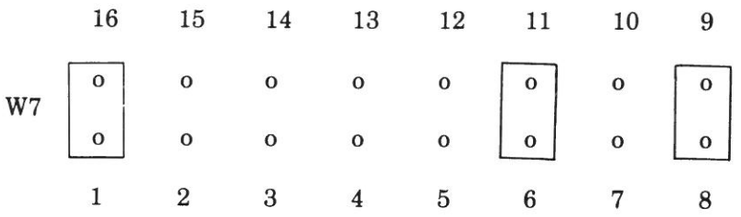
Throughout the manual, jumper locations are referenced by 'W' number and pin number. The following number convention is adhered to for all jumpers on the board.

For horizontal jumpers that are single row (1x3, 1x4, etc.), pins are numbered consecutively from left to right.

For vertical jumpers that are single row (1x3, 1x4, etc.), pins are numbered consecutively from top to bottom.

For horizontal jumpers that are dual row (2x3, 2x4, etc.), pins are numbered consecutively from bottom left to right, continuing on the top right to left.

EXAMPLE: W7(1), W7(6), and W7(8) are to be jumpered.



For vertical jumpers that are dual row (2x3, 2x4, etc.), pins are numbered consecutively from left top to bottom, continuing on the right bottom to top.

For horizontal jumpers that are triple row (3x3, 3x4, etc.), pins are numbered consecutively from left bottom to top, continuing from bottom to top for each column from left to right.

EXAMPLE: W3(4-5) is to be jumpered.