

# MORROW DESIGNS

## USER'S MANUAL

### SWITCHBOARD™

#### General Purpose Interface Board

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ADDENDUM (1)

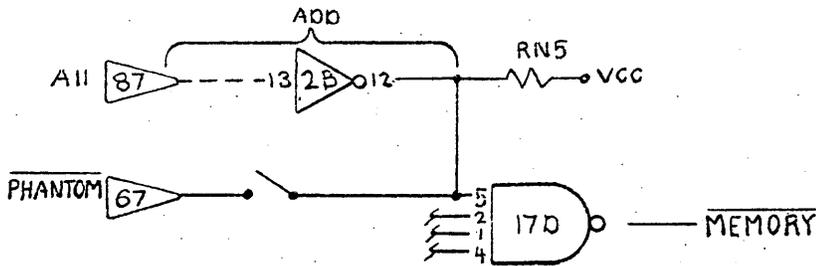
WARNING!

USERS OF REV 1 SWITCHBOARDS WHO HAVE BEEN ACCUSTOMED TO THE ORIGINAL SWITCHBOARD SHOULD BE EXTREMELY CAREFUL WHEN ATTACHING CABLES TO SERIAL DEVICE 1 ON CONNECTOR J1. PIN 3 ON J1 NOW HOLDS +12 VOLTS DC -- NOT RS-232 GROUND! OLD CABLE CONFIGURATIONS THAT WORK FINE ON PRE-REV 1 SWITCHBOARDS SHOULD BE DOUBLE CHECKED TO MAKE SURE THAT J1 PIN 3 IS NOT USED AS GROUND. CABLES WHICH USE PIN 4 AS RS-232 GROUND WILL WORK ON ALL REVISIONS. ALL CABLES SHOULD BE RETROFITTED TO USE PIN 4 AS GROUND TO AVOID MISHAPS.

# MORROW SWITCHBOARD MODS

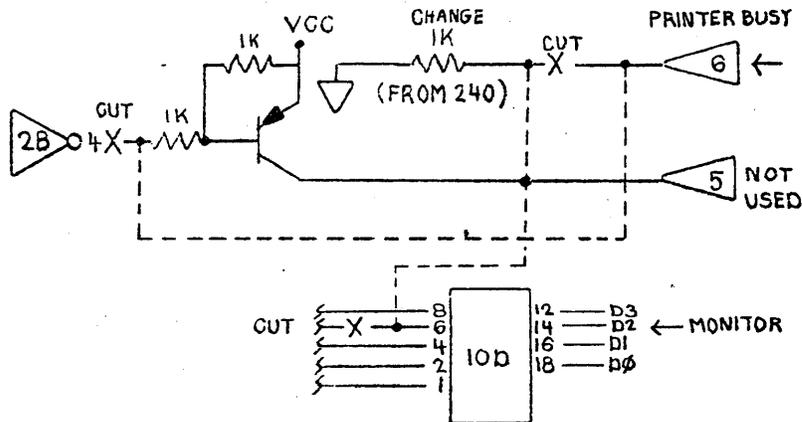
TO DISABLE 2K OF 4K EPROM OR RAM

(DISABLES 2ND 2K- OMITTING  
2B DISABLES 1ST 2K)



PERMITS ADDRESSING OF RAM/EPROM WITHIN  
SAME 4K BLOCK AS DISCUS ROM/RAM

TO MONITOR A PRINTER 'BUSY' LINE  
WHEN USING RS-232



MONITOR DATA BIT D2 ON PORT BASE+3.  
IF PRINTER BUSY, LOOK FOR LO TO PRINT.  
IF PRINTER BUSY, LOOK FOR HI TO PRINT.

1/ ADD TWO JUMPERS  
2/ CUT TWO TRACES

(D0, D1 OR D3 MAY ALSO BE USED IN WHICH  
CASE THE MOD SHOWN SHOULD BE MADE  
TO 10D- 2, 4 OR 8, RESPECTIVELY.

ATTENTION USERS OF THE NORTH STAR ZPB-2A PROCESSOR BOARD  
OR THE NORTH STAR DOUBLE DENSITY DISK CONTROLLER BOARD

WRITE DATA RACE CONDITION

A race condition exists in the write data logic of the ZPB-2A CPU board which can interfere with the operation of other boards on the bus if these boards utilize an internal bi-directional data bus. The following modification will alleviate this problem without degrading the performance of the North Star CPU or any other known device sharing the bus.

Locate IC F7. It is a 74LS132 in the upper left section of the ZPB circuit board. Remove this chip from its socket, bend out pin 10 and replace the IC in its socket in such a way that pin 10 sticks out without making contact with its assigned socket hole or with any other component. Make sure that the chip is oriented correctly. Pin 10 should be pointing toward the top of the board. This completes the modification.

PHANTOM LINE

A characteristic of the North Star double density disk controller board which may cause problems is that the PHANTOM line-- S-100 line 67-- is driven by an OPEN COLLECTOR device. It is therefore recommended that somewhere on the bus this line be pulled up through a suitable resistor (e.g. 3K, 1/4 Watt) to 5 volts. This modification is not necessary if the bus is actively terminated.

## INTRODUCTION

This board is packed! Until now, to get comparable performance it was necessary to buy at least two, and possibly three boards. Back when the 3P+S card was still available there were just enough lines for a bare bones interface to a 13-bit daisywheel printer. After slapping on a video terminal, where could you string the modem? That could go on a TU-ART board, but that left you with fewer slots, an extra UART and less money. Oh, well, any port in a storm...

Of course, you still didn't have a place to put some EPROM for a monitor or printer drivers or a bootstrap routine. Another board, another slot, another bill.

And if the EPROM card left you with, say, 1K of wasted address space, you soon found that 1K RAM boards are pretty hard to come by. Not even Godbout has 'em!

If only somebody could put all this stuff on one board! Somebody could. Somebody did. George Morrow has done it again!

With the Switchboard, instead of several good boards you can now have one great board. On a single S-100 card you get:

- \* Two fully independent RS232/TTY CURRENT LOOP serial ports with sixteen switch selectable baud rates, as well as switchable stop bit length, parity enable, parity odd/even, and seven or eight bit word length.
- \* One SERIAL STATUS port with four status bits for each serial port indicating receiver buffer full, transmitter buffer empty, parity error and over-run error.
- \* Four independent PARALLEL I/O ports: 32 lines switch selectable in groups of eight as input or latched output, with an attention status bit for each group of eight lines.
- \* One separate STATUS port with a latched attention bit for each parallel port, switch selectable to latch on a positive or negative pulse or level; with each attention status bit reset automatically by an input reference to its associated port.
- \* One separate STROBE port with eight independent 500 nanosecond strobe lines, each switch selectable as positive or negative strobe.
- \* Optional 4K of 2114 static RAM guaranteed to run at 4MHZ.
- \* PHANTOM DISABLE switch selection to allow PHANTOM line to disable on board RAM and EPROM.

AND

- \* Room for 4K of 2708 EPROM to boot! Wait states insertable!

## Introduction

### I/O MAP

#### IN

BASE.....SERIAL DEVICE 1, UART 3C  
BASE+1...SERIAL DEVICE 2, UART 4C  
BASE+2...SERIAL STATUS PORT  
BASE+3...ATTENTION STATUS PORT, 4 BITS EXTERNALLY SET  
BASE+4...PARALLEL PORT 1, RESETS BASE+3 BIT 0  
BASE+5...PARALLEL PORT 2, RESETS BASE+3 BIT 1  
BASE+6...PARALLEL PORT 3, RESETS BASE+3 BIT 2  
BASE+7...PARALLEL PORT 4, RESETS BASE+3 BIT 3 (pulled up)

#### OUT

BASE.....SERIAL DEVICE 1, UART 3C  
BASE+1...SERIAL DEVICE 2, UART 4C  
BASE+2...NOT USED  
BASE+3...STROBE PORT, STROBES 1 OF 8 EXTERNAL LINES  
BASE+4...PARALLEL PORT 1  
BASE+5...PARALLEL PORT 2  
BASE+6...PARALLEL PORT 3  
BASE+7...PARALLEL PORT 4 (pulled up)

(Parallel Port 4 data is pulled up to 5V with 3.3K resistors)

## OPERATING INSTRUCTIONS

### I/O ADDRESSING

The Switchboard contains eight I/O ports accessed by the IN "N" and OUT "N" instructions, where "N" is the number assigned to the port through the appropriate DIP switch setting. These eight ports can be thought of as a string of consecutive ports with fixed functions and fixed locations with respect to one another. The user determines the starting location of the whole string or block.

"BASE", the first, lowest port number on the board, can be any number beginning at 0 and continuing, in intervals of eight, up to 248. In other words, the lowest switch setting for "BASE" is 0, then 8, then 16 and so on.

Once "BASE" is determined, all eight port addresses are fixed. Thus, RS232C/TTY current loop serial ports 1 and 2 equal BASE and BASE+1 respectively; the serial status port equals BASE+2; the strobe and attention ports equal BASE+3; and the parallel ports equal BASE+4 through BASE+7. This order is illustrated in the table below:

S-100 I/O PORT NUMBER	SWITCHBOARD FUNCTION
BASE	SERIAL PORT 1
BASE+1	SERIAL PORT 2
BASE+2	SERIAL STATUS PORT
BASE+3	STROBE AND ATTENTION PORTS
BASE+4	PARALLEL PORT 1
BASE+5	PARALLEL PORT 2
BASE+6	PARALLEL PORT 3
BASE+7	PARALLEL PORT 4

Dip Switch 5 on the circuit board controls the address of serial port 1 or BASE, and hence, of all Switchboard I/O port addresses. Five of the paddles on Dip Switch 5 are used to determine the BASE address. Paddle 3 is associated with address bit 3, paddle 6 with address bit 4, paddle 2 with bit 5, paddle 4 with bit 6, and paddle 5 with bit 7.

Note that the paddles are not consecutive! The table provided below should be consulted when setting these switches. Address bits 0, 1 and 2 are not used here but are decoded elsewhere to determine the eight fixed ports which follow from the address of BASE.

To set BASE to 0, so that the eight I/O ports on The Switchboard occupy S-100 port numbers 0 through 7, all five paddles should be put in the "on" position. To set BASE to 248,

## Operating Instructions

all five paddles should be "off". Since there are 256 possible I/O device addresses on the S-100 bus, 32 starting locations are available for assigning The Switchboard I/O string. The following table shows the switch settings for all possible locations of BASE:

BASE ADDRESS			SWITCH SETTING				
Decimal	Hex	Octal	SW5-5 (A7)	SW5-4 (A6)	SW5-2 (A5)	SW5-6 (A4)	SW5-3 (A3)
0	00	000	on	on	on	on	on
8	08	010	on	on	on	on	off
16	10	020	on	on	on	off	on
24	18	030	on	on	on	off	off
32	20	040	on	on	off	on	on
40	28	050	on	on	off	on	off
48	30	060	on	on	off	off	on
56	38	070	on	on	off	off	off
64	40	100	on	off	on	on	on
72	48	110	on	off	on	on	off
80	50	120	on	off	on	off	on
88	58	130	on	off	on	off	off
96	60	140	on	off	off	on	on
104	68	150	on	off	off	on	off
112	70	160	on	off	off	off	on
120	78	170	on	off	off	off	off
128	80	200	off	on	on	on	on
136	88	210	off	on	on	on	off
144	90	220	off	on	on	off	on
152	98	230	off	on	on	off	off
160	A0	240	off	on	off	on	on
168	A8	250	off	on	off	on	off
176	B0	260	off	on	off	off	on
184	B8	270	off	on	off	off	off
192	C0	300	off	off	on	on	on
200	C8	310	off	off	on	on	off
208	D0	320	off	off	on	off	on
216	D8	330	off	off	on	off	off
224	E0	340	off	off	off	on	on
232	E8	350	off	off	off	on	off
240	F0	360	off	off	off	off	on
248	F8	370	off	off	off	off	off

As an example, to address a parallel port as S-100 I/O port 190 (BE Hex or 276 Octal), BASE would be set to 184, so that serial device 1 on The Switchboard would occupy I/O Port 184, serial device 2 would take Port 185, serial status would be accessed through Port 186 and so forth until the third parallel port on The Switchboard, which would be assigned the desired port number 190.

## Operating Instructions

Since a parallel port may only be assigned a number within the last four addresses in any eight port string, there is exactly a fifty-fifty probability that any arbitrarily chosen port number will actually be available on The Switchboard for a parallel device. The odds drop sharply for other port types, for instance a status port.

Of course, it is unusual to require that a specific device be assigned a specific port number. More often the requirement is that a device not be locked into a specific port address, so as not to interfere with less versatile hardware. Any port function provided on The Switchboard has at least 32 possible addresses. For those who absolutely must have, say, a serial device located at I/O port 5, and who cannot simply rewrite their I/O drivers, the Switchboard may not be suitable.

### Serial Ports 1 and 2

The Switchboard contains two Western Digital 1602 UARTS, which can be used to communicate with various RS232 and TTY serial devices such as terminals, printers and modems. The Switchboard can accommodate two such devices, one for each UART, and allows access to them through 8080 type CPU IN and OUT instructions directed to the first three I/O ports on the board.

Once BASE is set as detailed in the section on I/O addressing, Device BASE is the access to the the UART at location 3C on the circuit board, and Device BASE+1 is the access to the UART at 4C. Device BASE+2 holds the status of both UARTS.

UART 3C, device BASE, connects to the outside world via the first 8 pins of the 50-pin flat cable connector J1. J1 pin 1 is RS232 IN, pin 2 is RS232 OUT, and pin 4 is RS232 ground. J1 pin 8 is TTYIN+, pin 7 is TTYIN-, pin 5 is TTYOUT+ and pin 6 is TTYOUT-. The corresponding connections for UART 4C, Device BASE+1, are located on the same pins of the other 50-pin flat cable connector J2. Refer to the following diagram for detailed pinouts. Note that J1 pin 3 holds regulated +12 volts DC, while J2 pin 3 is ground.

	SERIAL PORT 1		SERIAL PORT 2	
	J1 CONNECTOR		J2 CONNECTOR	
C				
O	RS232IN	=1] [2= RS232OUT	RS232IN	=1] [2= RS232OUT
M				
S				
P	+12 V DC	=3] [4= RS232GND	RS232GND	=3] [4= RS232GND
I				
O				
D				
N	TTYOUT+	=5] [6= TTYOUT-	TTYOUT+	=5] [6= TTYOUT-
E				
N	TTYIN-	=7] [8= TTYIN+	TTYIN-	=7] [8= TTYIN+
T				

## Operating Instructions

An OUT BASE instruction will cause the byte stored in the CPU's accumulator to be processed by the 1602 UART at 3C and to appear as an RS232C signal stream at J1 pin 2 and in TTY 20ma current loop format at J1 pins 5 and 6. An IN BASE instruction will deposit into the accumulator the byte stored in UART 3C's Receive Buffer, which the UART has previously assembled from an RS232C stream received off J1 pin 1 or from TTY data taken off J1 pins 7 and 8. OUT BASE+1 and IN BASE+1 instructions will similarly move data through the UART at location 4C.

Switches are provided to condition the serial data according to the requirements of the user. Though not all options available on the 1602 UART are implemented, all of the most widely used configurations are offered. Through the appropriate switch settings, the user can determine: baud rate; word length; stop bit count; parity/no parity and even/odd parity.

### BAUD RATE SELECTION

Switch 2 at the lower left corner of The Switchboard controls the baud rates for both UARTS, that is, for Serial Device 1 and Serial Device 2. The lower four paddles, 1-4, control Serial Device 1 and the upper four, 5-8, control Serial Device 2. Sixteen separate baud rates, ranging from 50 to 19,200, may be selected for each UART. The UARTS need not operate at the same baud rate. The following table lists all possible switch settings for the two UARTS.

### BAUD RATE SWITCH SETTINGS

SERIAL PORT #1: I/O PORT BASE (SERIAL PORT #2: I/O PORT BASE+1)*				BAUD RATE
SW2-1 (SW2-5)	SW2-2 (SW2-6)	SW2-3 (SW2-7)	SW2-4 (SW2-8)	
on	on	on	on	50
on	on	on	off	75
on	on	off	on	110
on	on	off	off	134.5
on	off	on	on	150
on	off	on	off	300
on	off	off	on	600
on	off	off	off	1200
off	on	on	on	1800
off	on	on	off	2000
off	on	off	on	2400
off	on	off	off	3600
off	off	on	on	4800
off	off	on	off	7200
off	off	off	on	9600
off	off	off	off	19,200

\*Switches in parentheses apply to Serial Port #2

## Operating Instructions

### WORD LENGTH

Paddle 4 of Switch 1, the leftmost dip switch on the circuit board, controls data word length selection for Serial Device 1; paddle 2 does the same for Serial Device 2. Placing paddle 4 in the "on" position sets the word length for Serial Device 1 to 7 bits, while "off" fixes the word length to 8 bits. Paddle 3 has the same effect on word length for Serial Device 2.

Some serial devices, such as the Lear Siegler ADM3A, allow the user to specify a word length of 7 or 8 bits. With such a device, the corresponding word length must be selected on the Switchboard. Other devices, like the Hazeltine 1500, always use a word length of 8 with the eighth bit used as an optional parity bit. For a Hazeltine 1500, then, the Switchboard must always be set to a word length of 8, as well as to the proper parity, if any.

The table below gives the data bit selection settings for Switch 1 of the Switchboard:

WORD LENGTH SELECTION		
SERIAL DEVICE 1	SERIAL DEVICE 2	WORD LENGTH
SW1-4	SW1-3	
"on"	"on"	7 BITS
"off"	"off"	8 BITS

### STOP BIT COUNT

SW1-6 controls the number of stop bits, either one or two, which serial device 1 sends after each data word, and SW1-5 controls stop bit count for serial device 2. The "off" position will set the device to two stop bits, and the "on" position to one.

Most devices are extremely tolerant concerning stop bit setting. As a general rule, if a device fails to communicate with the Switchboard, it is not because the stop bit setting is incorrect.

# Operating Instructions

## PARITY

Refer to the following table for parity setting.

PARITY SWITCH SETTING		
SERIAL DEVICE 1 BASE	SERIAL DEVICE 2 BASE+1	
SW1-8	SW1-7	"off" = No Parity / "on" = Parity
SW1-2	SW1-1	"on" = Odd Parity / "off" = Even

## SERIAL STATUS PORT

The serial status port is accessed through an IN BASE+3 instruction. It can be used to synchronize communication between a serial device and a program. All status lines provided on the 1602 UART may be sampled by an IN BASE+2 instruction. These status lines are listed in the table below:

### STATUS LINES OF THE 1602 UART

TBRE	--	TRANSMIT BUFFER EMPTY
DR	--	RECEIVER BUFFER FULL
OE	--	OVER-RUN ERROR
PE	--	PARITY ERROR

The serial status port is divided into two 4 bit nibbles, the lower nibble containing the status of serial device 1, I/O Port BASE, and the upper nibble that of device 2, I/O Port BASE+1. The following illustration details the assignment of these status bits in the serial status port BASE+2:

Status for Serial Device 2		Status for Serial Device 1
	I/O PORT BASE+2 DATA BIT #	
	7 6 5 4 3 2 1 0	
TRANSMIT BUFFER EMPTY		PARITY ERROR
RECEIVER BUFFER FULL		OVER-RUN ERROR
OVER-RUN ERROR		RECEIVER BUFFER FULL
PARITY ERROR		TRANSMIT BUFF. EMPTY

## Operating Instructions

### SAMPLE SERIAL I/O IMPLEMENTATION

As an example of using the first three ports on the Switchboard, suppose we have a program which calls three I/O routines, labeled TIN, TOUT, and POUT. The following specifications apply for these routines:

TIN must get a character from a terminal device and return with the byte representing that character in the accumulator of the CPU. The 8th bit, data bit 7, must be cleared.

TOUT must send the byte contained in the B register of the CPU out to the terminal device and then return to the calling program.

POUT must output the byte contained in the B register to a printer and then return to the program.

For a terminal we will use a Hazeltine 1500 set at 9600 Baud, and for a printer we will use a Diablo 1610 with an RS232 interface and set at 300 Baud. For the sake of simplicity, parity will not be enabled on either I/O device or on the Switchboard.

The Hazeltine will be assigned as serial device 1 and addressed at I/O Port 0, while the Diablo will take what is left, namely serial device 2, I/O Port 1.

Three dip switches on the Switchboard are involved in this example. SW5, paddles 3 through 7, should all be in the "on" position in order to fix BASE to 0. This way the Hazeltine will occupy I/O Port BASE, or 0, and the Diablo BASE+1, or 1. The status port for both devices will be BASE+2, in this case I/O Port 2.

Dip Switch 2, which controls baud rate for serial devices 1 and 2, should have paddles 1, 2 and 3 "on" and 4 "off". This will set the baud rate for the Hazeltine, device 1, to 9600. Paddles 5 and 7 should be "on" while 6 and 8 should be "off" in order to put serial device 2, the Diablo, at 300 baud.

Since we are not using parity, it should be disabled on both the terminal and the printer as well as on the Switchboard. Thus on Dip Switch 1, paddles 7 and 8 should be "off" to inhibit parity. Paddle 4 on SW1, controlling word length select for serial device 1, should be "off" since the Hazeltine requires 8 bits. Were we using an ADM3A, we would have to make sure that paddle 4 was set to the same word length as the ADM3-- "on" for 7 bits and "off" for 8 bits.

Pin 1 of J1 on the Switchboard should be connected to pin 2 of the Hazeltine's EIA connector; pin 2 of J1 should go to pin 3 of the EIA connector; and pin 4 of J1 should go to the

## Operating Instructions

Hazeltine's pin 1. In addition, pins 1 and 7 of the EIA connector (protective ground and signal ground) should be tied together. Also, pins 7 and 8 of J1 should be jumpered together to bring -12V from the TTYIN- line to the RS232 circuit.

J2 of the Switchboard and the EIA connector of the Diablo printer should be connected according to the same scheme, which is depicted below:

J1 or J2 Pin Number	EIA Connector Pin Number
1.....	2
2.....	3
4.....	1,7
7 tied to 8	NC

-----  
 | WHEN USING EITHER SERIAL PORT WITH AN RS232 DEVICE, THE TTYIN- |  
AND TTYIN+ LINES OF THAT SERIAL PORT MUST BE JUMPERED TOGETHER!

Our sample routines could then be implemented as follows:

### TIN ROUTINE

(Input data from serial device 1 into accumulator)

Octal	Hex	
100:000 333 002	4000 DB 02	TIN IN 2 GET STATUS BYTE
002 346 004	4002 E6 04	ANI 4 STRIP DR DEVICE 1
004 312 000 100	4004 CA 00 40	JZ TIN TEST FOR DR
007 333 000	4007 DB 00	IN 0 GET DEVICE 1 DATA
011 346 177	4009 E6 7F	ANI 127 STRIP OFF 8TH BIT
013 311	400B C9	RET RETURN

### TOUT ROUTINE

(Output data from register B to serial device 1)

100:100 333 002	4040 DB 02	TOUT IN 2 GET STATUS BYTE
102 346 010	4042 E6 08	ANI 8 STRIP TBRE DEV. 1
104 312 100 100	4044 CA 40 40	JZ TOUT TEST FOR TBRE
107 170	4047 78	MOV A,B DATA TO ACC
110 323 000	4048 D3 00	OUT 0 TRANSMIT TO DEV. 1
112 311	404A C9	RET

### POUT ROUTINE

(Output data from register B to serial device 2)

100:200 333 002	4080 DB 02	POUT IN 2 GET STATUS BYTE
202 346 200	4082 E6 80	ANI 80H STRIP TBRE DEV. 2
204 312 200 100	4084 CA 80 40	JZ POUT TEST FOR TBRE
207 170	4087 78	MOV A,B DATA TO ACC
210 323 001	4088 D3	OUT 1 TRANSMIT TO DEV. 2
212 311	408A C9	RET

## Operating Instructions

### PARALLEL PORTS 1 TO 4

The Switchboard provides 32 lines of I/O divided logically into four 8 bit parallel ports, each of which can be DIP switch selected for input or latched output. Another separate port provides 4 latched attention status bits, one for each parallel port. The four parallel ports can be accessed by I/O instructions addressed to ports BASE+4, BASE+5, BASE+6, and BASE+7. Each port can be an input port or a latched output port but not both. Parallel port 4 (I/O port BASE+7) has its data lines pulled up to 5V through 3.3K Ohms for interfacing with open collector devices. Often the strobe signals, as opposed to data signals, of peripheral devices such as printers require pull ups.

If a parallel port is set for input, then an IN BASE+3+N instruction will cause the data on the eight corresponding pins of J1 or J2, the 50 pin cable connectors on the top of the board, to be transferred to the accumulator of the CPU. In this case "N" is the number, 1-4, of the parallel port. The determination of BASE has been described earlier under "ADDRESSING".

If a parallel port is set for output, an OUT BASE+3+N instruction will cause the data in the accumulator to be latched on to the same pins of the J1 or J2 connector that would have been read by an IN instruction directed to that port number. Since the data is latched, it will remain on those pins until changed by a following OUT instruction.

Furthermore, A PARALLEL OUTPUT PORT CAN ALWAYS BE READ BY AN INPUT INSTRUCTION ADDRESSED TO THAT PORT. This can be very useful. It means that each output port can be used as a single byte of RAM memory completely outside of normal memory address space. Also, the last byte transmitted from that port can be checked non-destructively at any time simply by issuing an IN instruction to that port.

## Operating Instructions

There follows a list of pin assignments on J1 and J2, the two 50 pin flat cable connectors on the top of the Switchboard, for the four parallel ports.

### J1, J2 CONNECTIONS FOR PARALLEL PORTS 1-4

BIT #	BASE+4 PORT # 1	BASE+5 PORT# 2	BASE+6 PORT# 3	BASE+7 PORT# 4
0	J2-33	J1-49	J1-33	J2-49
1	J2-25	J1-41	J1-25	J2-41
2	J2-35	J1-50	J1-35	J2-50
3	J2-27	J1-43	J1-27	J2-43
4	J2-29	J1-45	J1-29	J2-45
5	J2-21	J1-37	J1-21	J2-37
6	J2-31	J1-47	J1-31	J2-47
7	J2-23	J1-39	J1-23	J2-39

### PARALLEL OUTPUT ENABLE

Each parallel port has associated with it a switch to determine whether it will be used as input or latched output. The first four paddles of DIP switch 4, the third DIP switch from the right on the top row of four switches, are the OUTPUT ENABLE switches. SW4-3 controls parallel port 1, SW4-2 parallel port 2, SW4-1 port 3, and SW4-4 port 4. Setting one of these switches to "on" will convert the port it controls into an output port, while setting it to "off" will make the port an input port. This is illustrated below.

### DESIGNATING PARALLEL PORTS AS INPUT OR OUTPUT ("on"=OUTPUT "off"=INPUT)

I/O PORT BASE+4 PARALLEL PORT#1	I/O PORT BASE+5 PARALLEL PORT#2	I/O PORT BASE+6 PARALLEL PORT#3	I/O PORT BASE+7 PARALLEL PORT#4 (pulled-up)
SW4-3	SW4-2	SW4-1	SW4-4

## Operating Instructions

### ATTENTION PORT

An attention port is provided on the Switchboard at I/O port address BASE+3 that allows an external device to set a flag which the CPU can read and which the CPU automatically resets by the execution of an IN N instruction, where N is the I/O port number assigned to the parallel port associated with the flag bit.

The four low order bits of Switchboard I/O port BASE+3 can be set by an external device by strobing a designated pin on J1 or J2, the two 50 pin ribbon cable connectors on the top of the Switchboard. The polarity of the strobe can be set by a DIP switch on the board. An external device strobing J2-17 will set bit 0 of Attention Port BASE+3; strobing J1-19 will set bit 1; strobing J1-17 will set bit 2 and strobing J2-19 will set bit 3. These bits can be sampled with an IN BASE+3 instruction.

#### ATTENTION PORT BASE+3 AND J1, J2 STROBE PINS

BIT 3...J2-19    BIT 2...J1-17    BIT 1...J1-19    BIT 0...J2-17

The external strobes can trigger their assigned attention port bit on a positive or negative strobe or level, depending on the setting of DIP switch 4, paddles 5 to 8. A paddle in the "on" position will cause triggering on a positive to negative transition. In the "off" position triggering will occur on a negative to positive transition. The following table outlines the relation between the polarity switches on SW4 and their respective attention port bit.

#### ATTENTION PORT BASE+3 AND POLARITY SWITCHES ("on"=Positive To Negative Transition) ("off"=Negative to Positive Transition)

BIT 3...SW4-6    BIT 2...SW4-7    BIT 1...SW4-5    BIT 0...SW4-8

### AUTOMATIC RESET OF ATTENTION BIT

Each attention strobe pin and its corresponding bit in attention port BASE+3 has a special tie to a unique parallel port. Specifically, when a parallel port is addressed by an IN N instruction, where N is the I/O port number assigned to the parallel port, the attention bit associated with that port is automatically reset.

Thus, if BASE is made 0, thereby assigning parallel port 2 the I/O device number of 5, then strobing J1-19, its associated

## Operating Instructions

strobe pin, will set to a logical "1" bit 1 of I/O port 3, its associated attention port flag bit. An IN 5 instruction will, in this case, reset I/O port 3, bit 1. The complete logical correspondence of strobe pin number, polarity select bit, attention port bit, and parallel port number is delineated below.

STROBE PIN	POLARITY SWITCH	ATTENTION PORT BIT	PARALLEL PORT # (I/O PORT BASE+3)
J2-17	SW4-8	0	(1) BASE+4
J1-19	SW4-5	1	(2) BASE+5
J1-17	SW4-7	2	(3) BASE+6
J2-19	SW4-6	3	(4) BASE+7

### STROBE PORT BASE+3

An OUT BASE+3 instruction will cause a 500 nano-second strobe to appear on one of eight pins on the J1 or J2 connectors at the top of the Switchboard. The pin that outputs the strobe is selected by the bit pattern formed by bits 0, 1 and 2 in the accumulator at the time the OUT BASE+3 instruction is executed. The polarity of the strobe for each pin is individually determined by setting the 8 paddles on DIP switch 3.

The "on" position will cause its associated pin to rest at ground until it is strobed, whereupon it will go high for 500 nanoseconds on an 8080 based system, 700 nseconds on a Z-80 running at 2 MHZ and 350nseconds on a 4MHZ Z-80. The "off" position will produce a positive quiescent state which strobes negative. The correspondence among BASE+3 data bits, J1 and J2 connector pin number, and DIP switch 3 paddle is detailed below.

### STROBE PORT BASE+3 MAP

OUT STROBE PIN NUMBER	POLARITY SWITCH ON=POS., OFF=NEG.	STROBE PORT BASE+3 BIT PATTERN		
		BIT 2	BIT 1	BIT 0
J1-15	SW3-1	0	0	0
J1-11	SW3-2	0	0	1
J1-13	SW3-3	0	1	0
J1-9	SW3-4	0	1	1
J2-15	SW3-5	1	0	0
J2-11	SW3-6	1	0	1
J2-13	SW3-7	1	1	0
J2-9	SW3-8	1	1	1

## Operating Instructions

Thus if we wish to place a strobe with a positive going leading edge on J2 pin 13, we would first set SW3 paddle 7 to "on", then deposit a 6 in the accumulator, and finally execute an OUT BASE+3 instruction. Bits 3 through 7 are thrown away, so any byte with Bit 1 and 2 set and Bit 0 cleared would do the trick in our example.

### EPROM OPTION

The Switchboard has room for a block of four 2708 1K by 8 EPROM's, addressable on any 4K boundary. Two DIP switches, SW-5 and SW-6, have paddles which control three distinct functions concerning the EPROM: ROM disable, ROM address, and PHANTOM memory enable. This latter function is shared with the on board RAM memory option.

### EPROM ADDRESSING

Paddles 5 through 8 on DIP switch 6, in the upper right corner of the board, control EPROM addressing by determining the starting location of the 4K block of memory the EPROM is to occupy. If the EPROM block is enabled, the 4K block of memory to which it is addressed may not be utilized by off board memory except through the PHANTOM line. This is the case even if only 1 or 2 or 3K of EPROM is actually inserted on the Switchboard. In other words, if 1K of EPROM is used beginning at location 0000H, it is not permissible to address another memory board to begin one thousand bytes up at 0400H.

However, one need not lose that 3K of address space. The Switchboard RAM option, if addressed to the same starting location as the EPROM, may be used to fill any and all 1K gaps left by the EPROM, as long as those gaps begin on an even 1K boundary. In fact, EPROM and RAM may interweaved in 1K segments so that, for example, the first 1K of a 4K block could be EPROM, the next 2K RAM, and the last 1K EPROM again.

As with other series of switches on the Switchboard, these paddles are not sequential and it is recommended that the addressing table below be consulted when addressing EPROM.

## Operating Instructions

EPROM STARTING ADDRESS		DIP SWITCH SETTING			
HEX	OCTAL	SW6-5 (A15)	SW6-8 (A14)	SW6-7 (A13)	SW6-6 (A12)
0000	000:000	"on"	"on"	"on"	"on"
1000	020:000	"on"	"on"	"on"	"off"
2000	040:000	"on"	"on"	"off"	"on"
3000	060:000	"on"	"on"	"off"	"off"
4000	100:000	"on"	"off"	"on"	"on"
5000	120:000	"on"	"off"	"on"	"off"
6000	140:000	"on"	"off"	"off"	"on"
7000	160:000	"on"	"off"	"off"	"off"
8000	200:000	"off"	"on"	"on"	"on"
9000	220:000	"off"	"on"	"on"	"off"
A000	240:000	"off"	"on"	"off"	"on"
B000	260:000	"off"	"on"	"off"	"off"
C000	300:000	"off"	"off"	"on"	"on"
D000	320:000	"off"	"off"	"on"	"off"
E000	340:000	"off"	"off"	"off"	"on"
F000	360:000	"off"	"off"	"off"	"off"

Once a starting address for EPROM is selected, the 24 pin DIP socket at location 8E, the right most 24 pin socket on the Switchboard, can hold the first 1K chip in the block. Then adjacent sockets to the left can hold the second K, third K and fourth K in that order from right to left.

### EPROM ADDRESSING EXAMPLE

As an example, if only 1K of EPROM is required, and it is to begin at memory location DCO0H or 334:000Q, then the starting block for the EPROM should be set according to the above list to D000H (320:000Q). That is, SW-6 paddles 5, 6 and 8 should be "off" and paddle 7 should be "on". Also a programmed 2708 chip should be inserted in IC socket 4E, the socket just to the right of SW2 in the lower left corner of the board. This would cause the EPROM to occupy the fourth 1K of the 4K block beginning at D000H, which would indeed put it at DCO0H.

### ROM DISABLE

DIP switch 5, paddle 7, is the ROM disable switch. If it is in the "on" position the EPROM is functionally removed from the bus, regardless of its address. "Off" enables the EPROM.

### PHANTOM ENABLE

The first paddle on DIP switch 5, the second DIP switch from the upper right corner of the board, enables the PHANTOM line on the S-100 bus (pin #67). This signal is used to disable normal "slave" devices-- such as are available on the Switchboard-- in

## Operating Instructions

order to activate "phantom slave" devices for special circumstances. If your machine utilizes phantom devices, SW5-1 should be "on", and if not it should be "off".

### INSERTING WAIT STATES WHEN ADDRESSING EPROM

Due to the speed limitation of the 2708 EPROM, the EPROM option on the Switchboard is not guaranteed to function properly over all temperature ranges at 4 MHz. For this reason, a facility has been provided whereby the user can cause the Switchboard to insert "Wait States" whenever its on-board EPROM is being accessed. This option is selected by installing a jumper at location 4E on the Switchboard, just below the leftmost EPROM on the board.

At location 4E is a line of three plated through holes marked, from left to right, "X", "RDY", and "P". If the CPU card in the user's system responds to PREADY (S-100 line 72), then a jumper should be placed so as to connect the plated through hole marked "RDY" (the hole in the middle) with the hole to its right marked "P". If the CPU responds to "XRDY" (S-100 line 3), then the hole marked "RDY" should be jumpered to the hole marked "X". In either case, these jumpers will cause the ready line (3 or 72) to be asserted during a cycle in which on-board EPROM is being addressed. This jumper option insures that the 2708 EPROM will function properly in a 4 MHz system with a slight penalty in speed.

If the Switchboard is being run at 2 MHz, then no jumpering is necessary.

The "WAIT" option is illustrated below:

jumper X-RDY for		RDY		jumper RDY-P for
wait state on	*	*	*	wait state on
XRDY (S-100 line 3)	X		P	PRDY (S-100 line 72)

### RAM OPTION

The Switchboard has room for eight 2114-3 4K by 1 RAM's, available as an option from Thinker Toys. The 2114-3 chip is guaranteed to operate at 4 MHz. Any 2114 type chip which is functioning properly will run on the Switchboard at 2MHz. Note that to deposit into the Switchboard RAM from a front panel, the panel MUST generate the S-100 status signal SW0.

As with the EPROM option, Switchboard RAM is addressed as a 4K block beginning at the start of any 4K boundary and can fill the block in 1K segments which need not be consecutive and need not start at the first segment. If the 4K block of RAM is addressed to begin at the same location as the 4K block of EPROM, the RAM and EPROM can be interleaved in any combination of 1K

## Operating Instructions

segments as long as no 1K segment is shared by RAM and EPROM. The RAM may be enabled or disabled as a 4K block by setting a hardware switch and can also be disabled by the PHANTOM line if the PHANTOM ENABLE switch, described above, is set.

### RAM ADDRESSING

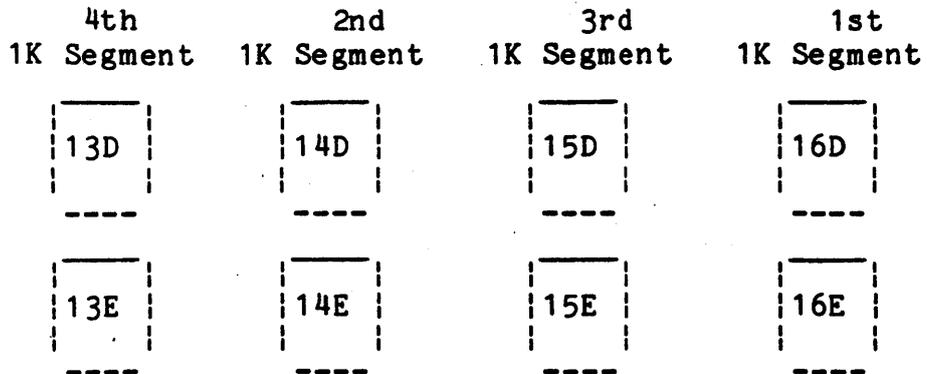
The first four paddles of DIP switch 6, in the upper right corner of the Switchboard, control RAM addressing. As with EPROM addressing, these switches establish the starting location of a 4K block of address space. The settings for all possible starting locations of this 4K block is given below. Again, for best results, refer to the chart.

RAM STARTING ADDRESS		SWITCH SETTING			
HEX	OCTAL	SW6-1 (A15)	SW6-4 (A14)	SW6-3 (A13)	SW6-2 (A12)
0000	000:000	"on"	"on"	"on"	"on"
1000	020:000	"on"	"on"	"on"	"off"
2000	040:000	"on"	"on"	"off"	"on"
3000	060:000	"on"	"on"	"off"	"off"
4000	100:000	"on"	"off"	"on"	"on"
5000	120:000	"on"	"off"	"on"	"off"
6000	140:000	"on"	"off"	"off"	"on"
7000	160:000	"on"	"off"	"off"	"off"
8000	200:000	"off"	"on"	"on"	"on"
9000	220:000	"off"	"on"	"on"	"off"
A000	240:000	"off"	"on"	"off"	"on"
B000	260:000	"off"	"on"	"off"	"off"
C000	300:000	"off"	"off"	"on"	"on"
D000	320:000	"off"	"off"	"on"	"off"
E000	340:000	"off"	"off"	"off"	"on"
F000	360:000	"off"	"off"	"off"	"off"

Since the 2114 RAM chip is a 1K by 4 array, it takes two chips to fill 1K of memory, the minimum amount that can be used on the Switchboard. Unlike the sockets provided for the EPROM, those provided for the RAM are not arranged sequentially. The four separate 1K segments are paired vertically on the board but do not follow in a straight right to left ascending order as do the EPROM sockets. The first 1K of RAM in the 4K block goes into the two 18 pin sockets at 16E and 16D, near the lower right corner of the Switchboard. The second 1K segment goes into 14E and 14D, two columns over from the first segment. The third 1K block goes into 15E and 15D, while the last segment goes into 13E and 13D. This is illustrated below.

## Operating Instructions

### PHYSICAL LOCATION OF 1K RAM SEGMENTS ON CIRCUIT BOARD



### RAM ADDRESSING EXAMPLE

Suppose we have placed 1K of EPROM on the Switchboard at DCOOH, or 334:000Q, and want to fill the rest of the 4K address space with RAM. First, address the RAM to start at the same location as the EPROM, namely, D000H or 320:000Q. For the RAM, this would involve setting SW-6 paddles 1, 2 and 4 "off" and paddle 3 "on", as per the above chart. Next, take six 2114 RAM chips and place them in sockets 14D and E, 15D and E, and 16 D and E. If the EPROM is properly addressed and if an EPROM is inserted in socket 4E, we should now have a single 4K block filled with 3K of RAM at the bottom and 1K of EPROM at the top.

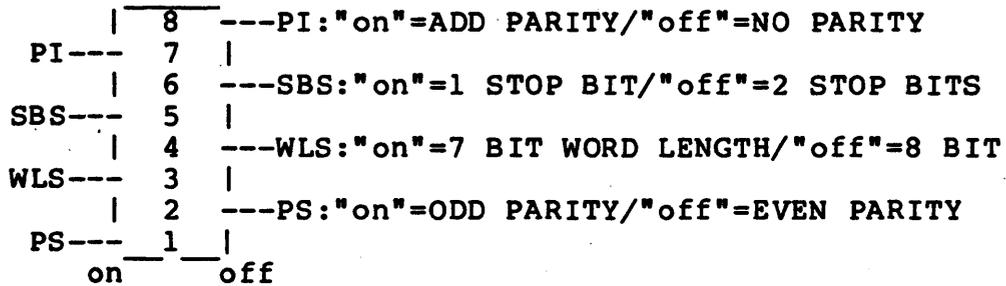
### RAM DISABLE

Putting paddle 8 of DIP switch 5 in the "on" position removes the Switchboard RAM from the bus. This will free up whatever address the RAM was set to occupy for use by other boards in the computer unless the Switchboard EPROM shares the same location. In this case the EPROM will occupy the 4K block in question by itself-- unless, of course, it too is disabled.

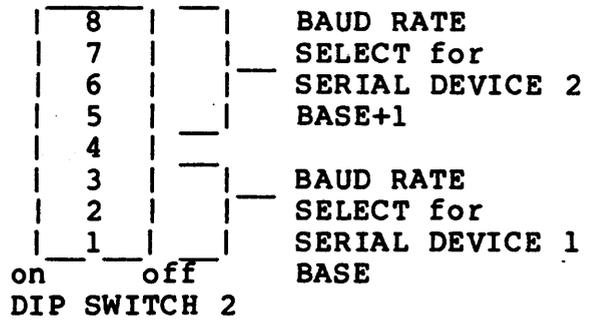
**BIRD'S EYE VIEW OF SWITCHBOARD  
DIP SWITCHES AND THEIR FUNCTIONS**

UART 4C  
SERIAL DEVICE 2  
BASE+1

UART 3C  
SERIAL DEVICE 1  
BASE



DIP SWITCH 1  
-----  
left most switch  
2C



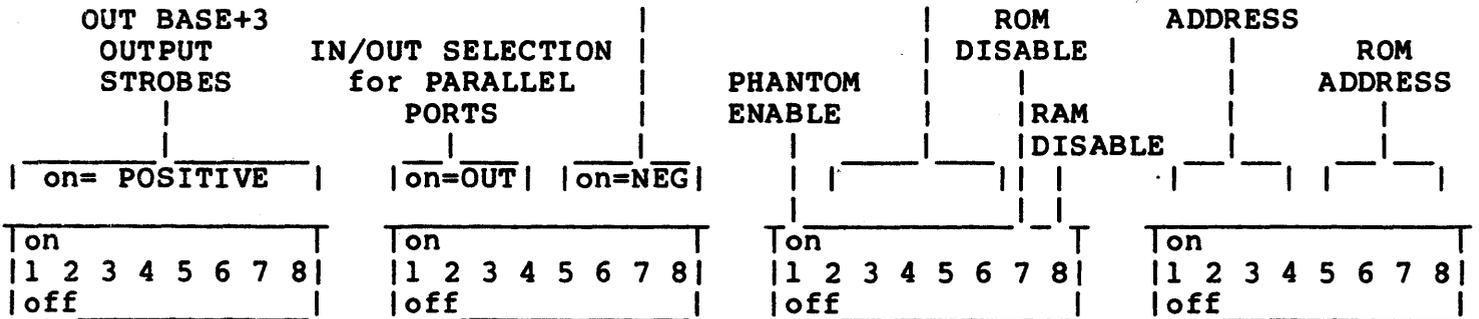
lowest switch  
3E

POLARITY  
SELECT for  
IN BASE+3  
ATTENTION STATUS  
PORT

POLARITY  
SELECT for

I/O  
ADDRESS

RAM



DIP SWITCH 3  
-----  
A10-11

DIP SWITCH 4  
-----  
A12-13

DIP SWITCH 5  
-----  
A14-15

DIP SWITCH 6  
-----  
right most switch  
A16-17

PIN ASSIGNMENTS FOR 50 PIN RIBBON CABLE CONNECTORS J1 AND J2

J1

(left connector)

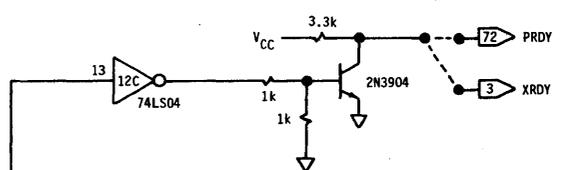
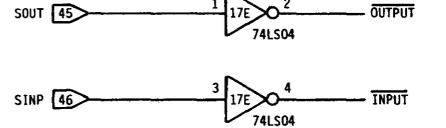
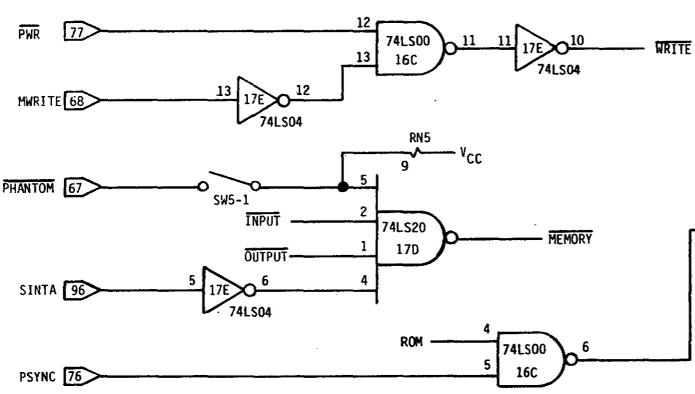
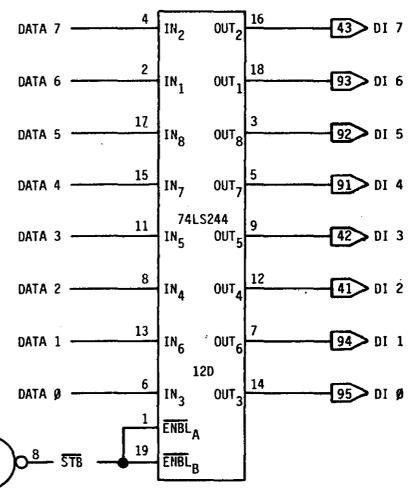
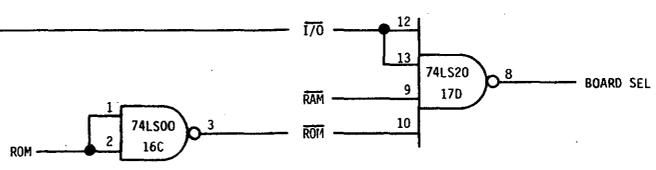
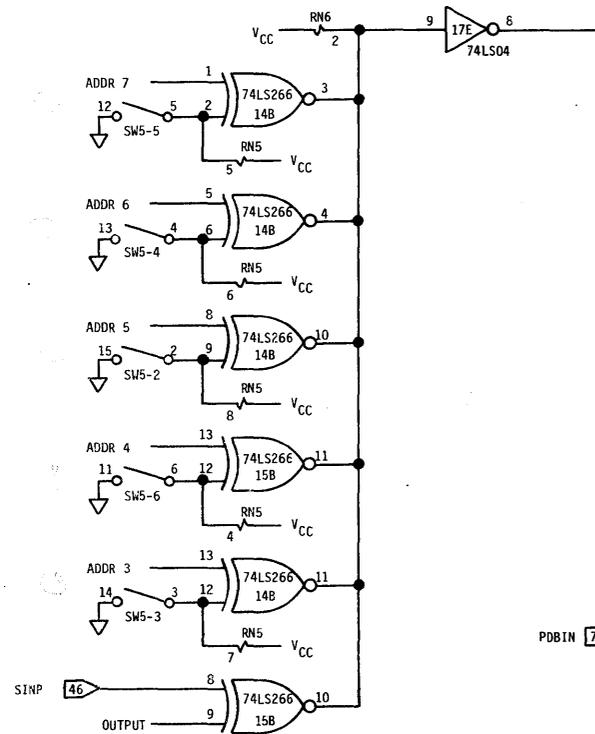
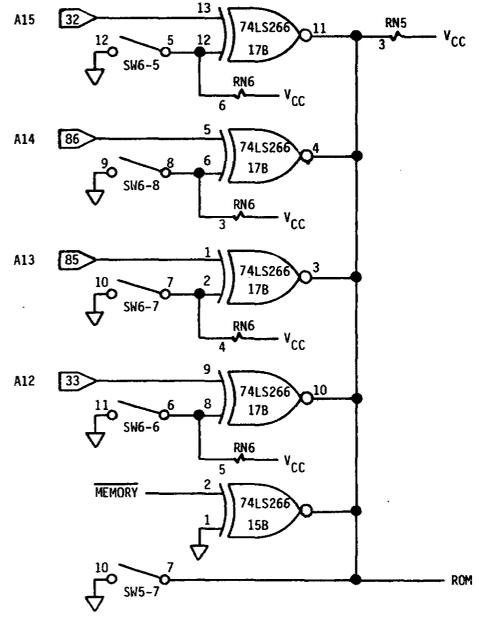
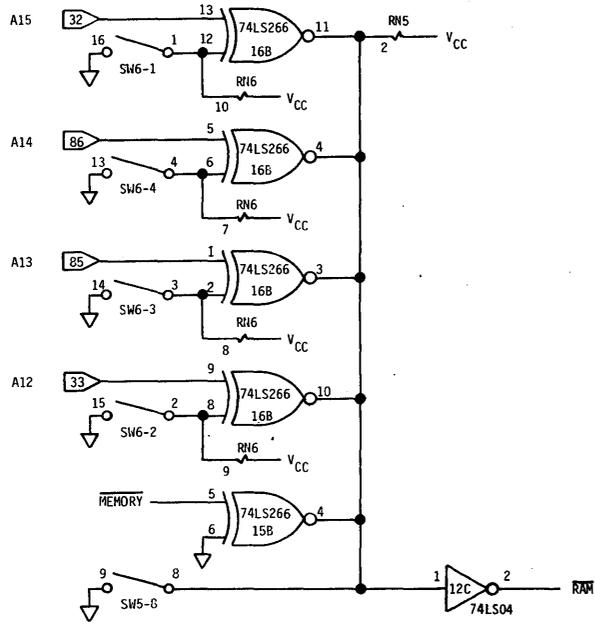
Function	Pin #	Function
RS232IN A=1		2=RS232OUT A
+12V DC=3		4=RS232GND A
TTYOUT+ A=5		6=TTYOUT- A
TTYIN- A=7		8=TTYIN+ A
STB-D=9		10=GND
STB-B=11		12=GND
STB-C=13		14=GND
STB-A=15		16=GND
ATN STB G=17		18=GND
ATN STB F=19		20=GND
DATA 5 G=21		22=GND
DATA 7 G=23		24=GND
DATA 1 G=25		26=GND
DATA 3 G=27		28=GND
DATA 4 G=29		30=GND
DATA 6 G=31		32=GND
DATA 0 G=33		34=GND
DATA 2 G=35		36=GND
DATA 5 F=37		38=GND
DATA 7 F=39		40=GND
DATA 1 F=41		42=GND
DATA 3 F=43		44=GND
DATA 4 F=45		46=GND
DATA 6 F=47		48=GND
DATA 0 F=49		50=DATA 2 F

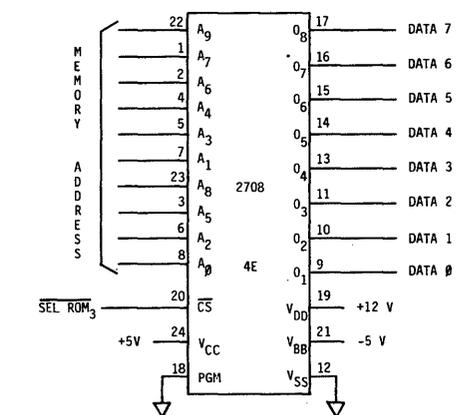
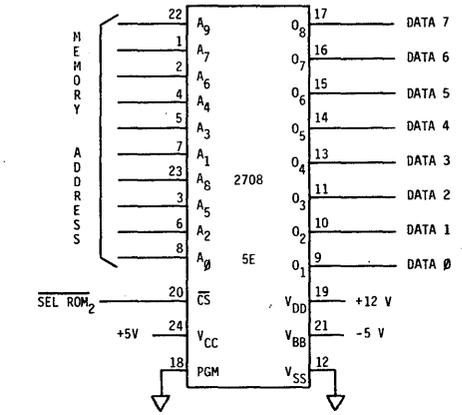
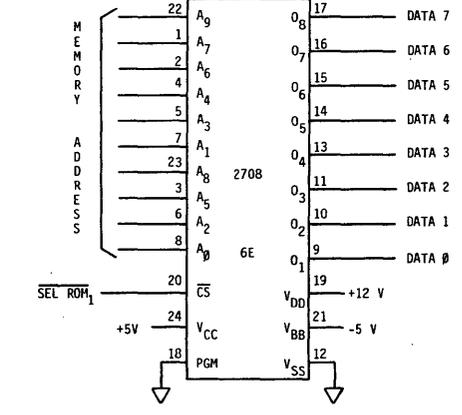
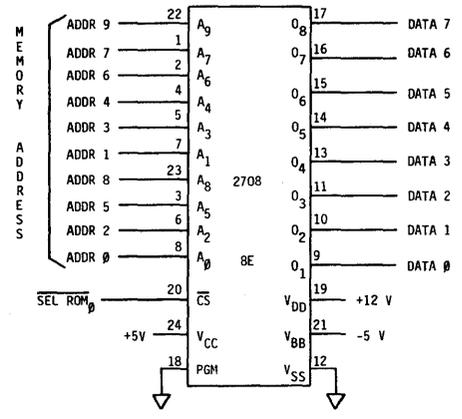
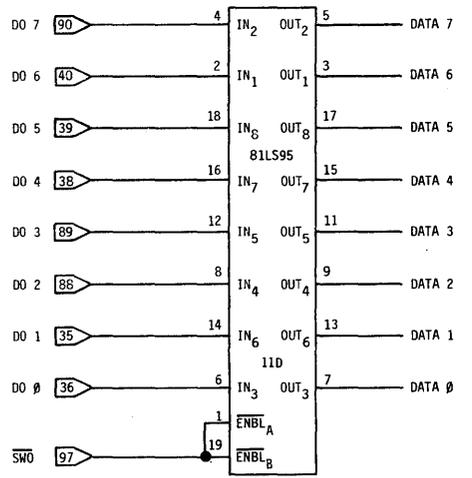
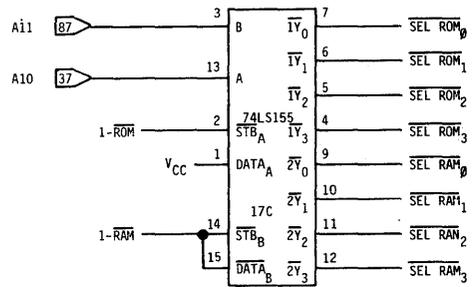
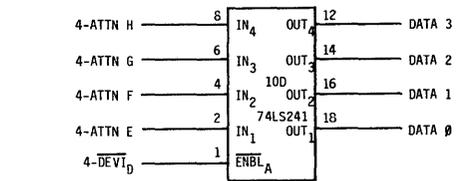
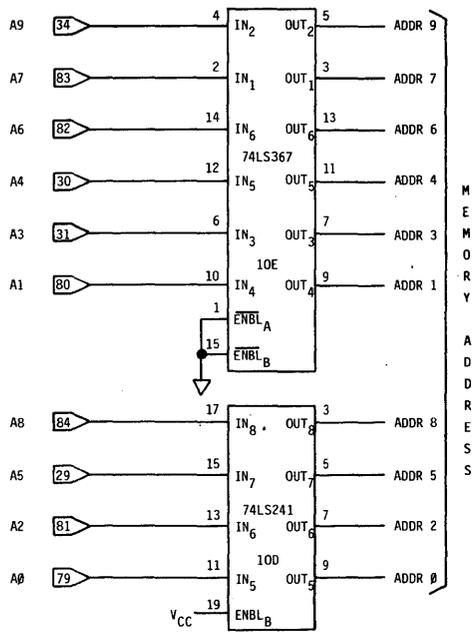
J2

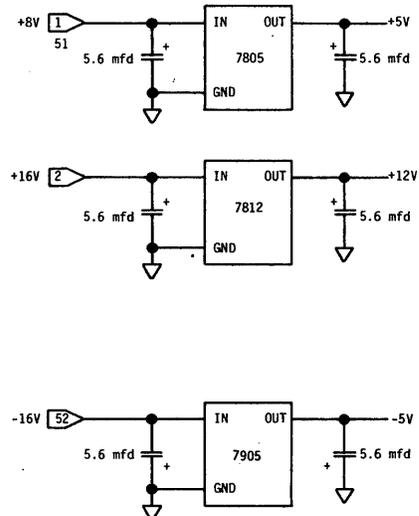
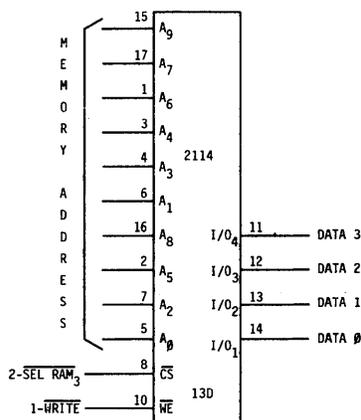
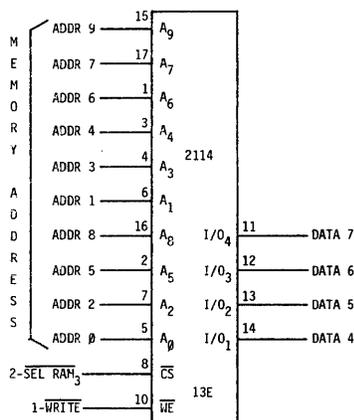
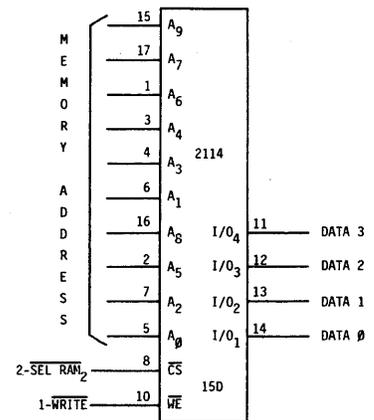
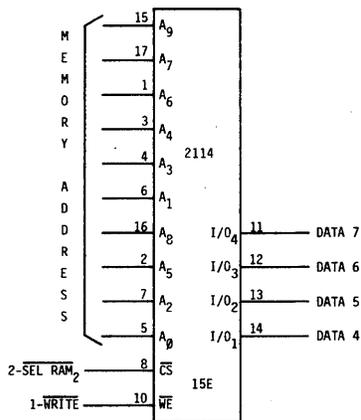
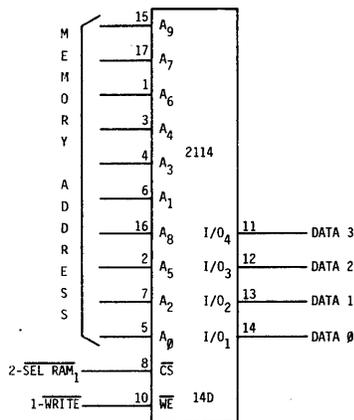
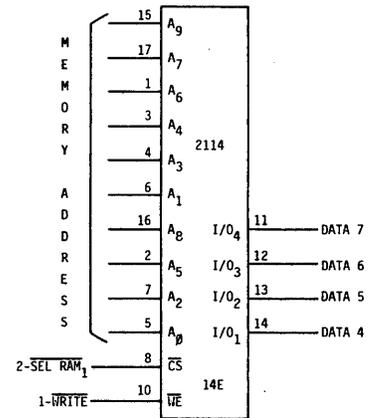
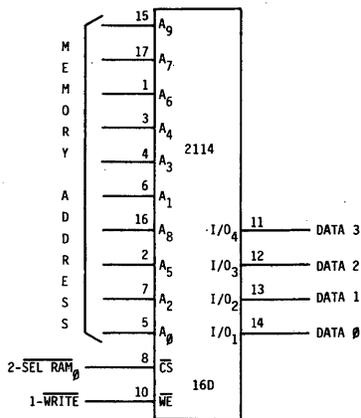
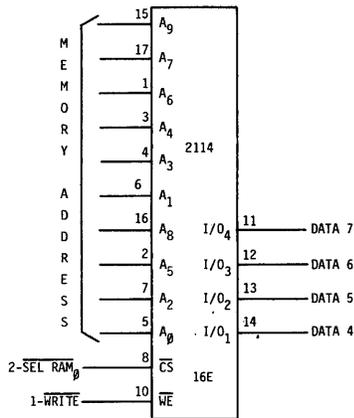
(right connector)

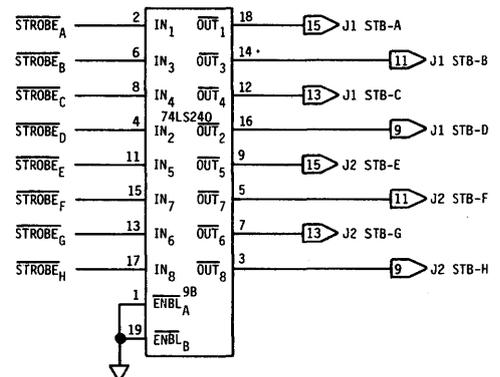
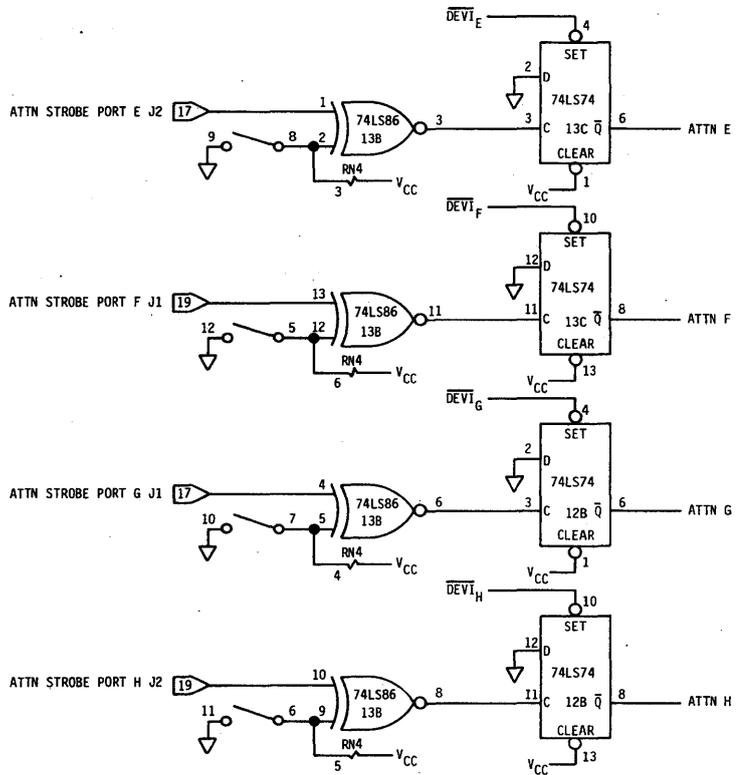
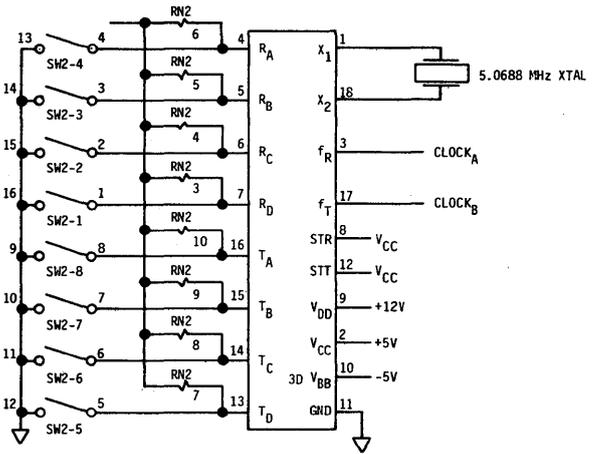
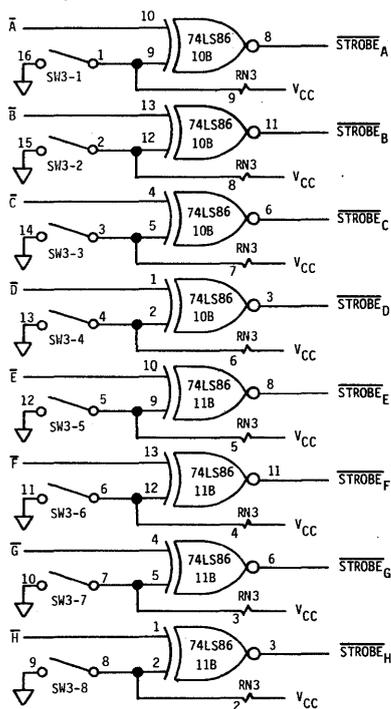
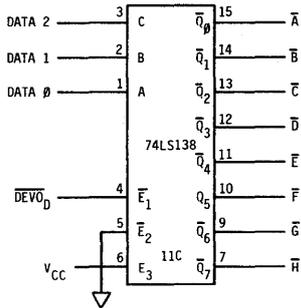
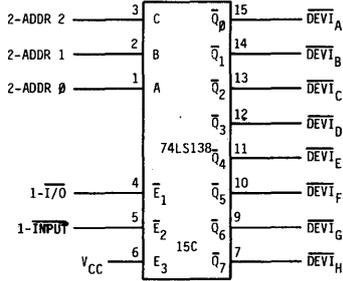
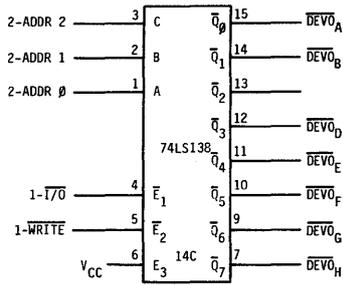
Function	Pin #	Function
RS232IN B=1		2=RS232OUT B
RS232GND B=3		4=RS232GND B
TTYOUT+ B=5		6=TTYOUT- B
TTYIN- B=7		8=TTYIN+ B
STB-H=9		10=GND
STB-F=11		12=GND
STB-G=13		14=GND
STB-E=15		16=GND
ATN STB E=17		18=GND
ATN STB H=19		20=GND
DATA 5 E=21		22=GND
DATA 7 E=23		24=GND
DATA 1 E=25		26=GND
DATA 3 E=27		28=GND
DATA 4 E=29		30=GND
DATA 6 E=31		32=GND
DATA 0 E=33		34=GND
DATA 2 E=35		36=GND
DATA 5 H=37		38=GND
DATA 7 H=39		40=GND
DATA 1 H=41		42=GND
DATA 3 H=43		44=GND
DATA 4 H=45		46=GND
DATA 6 H=47		48=GND
DATA 0 H=49		50=DATA 2 H

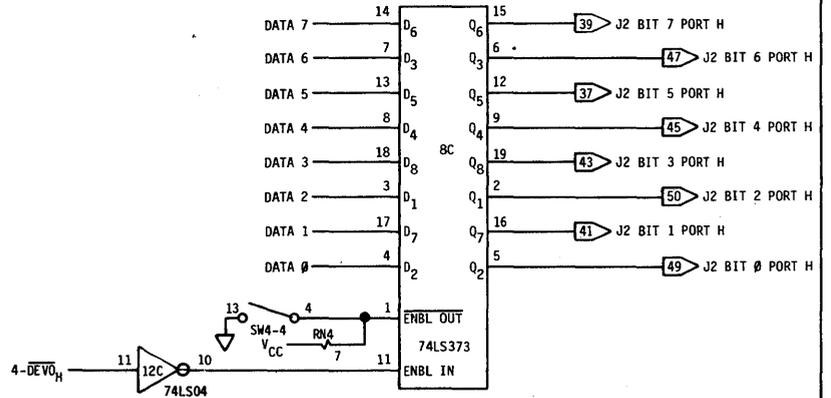
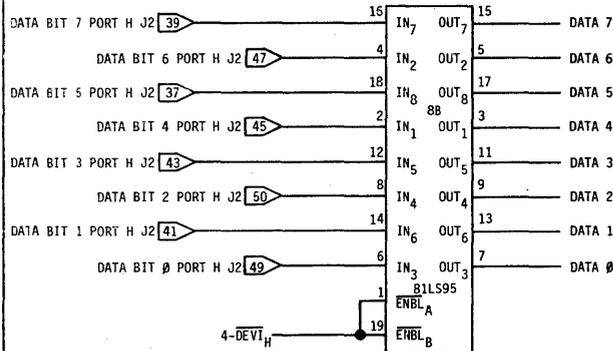
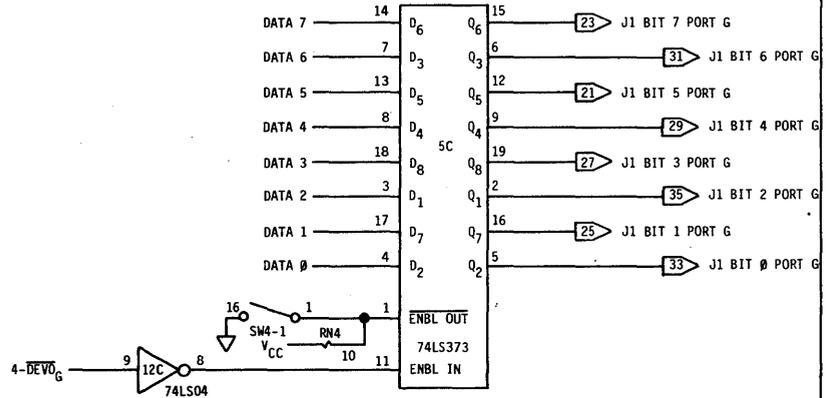
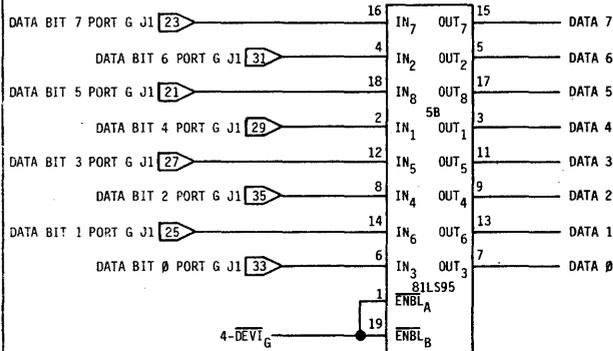
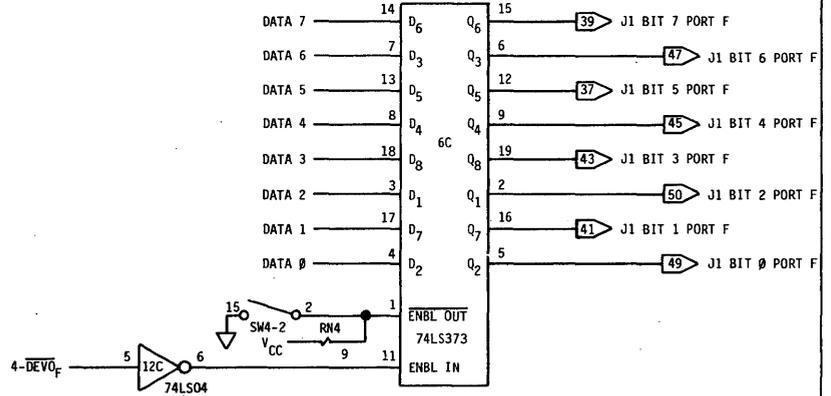
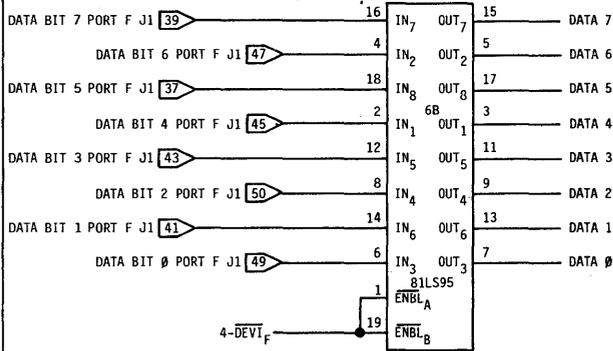
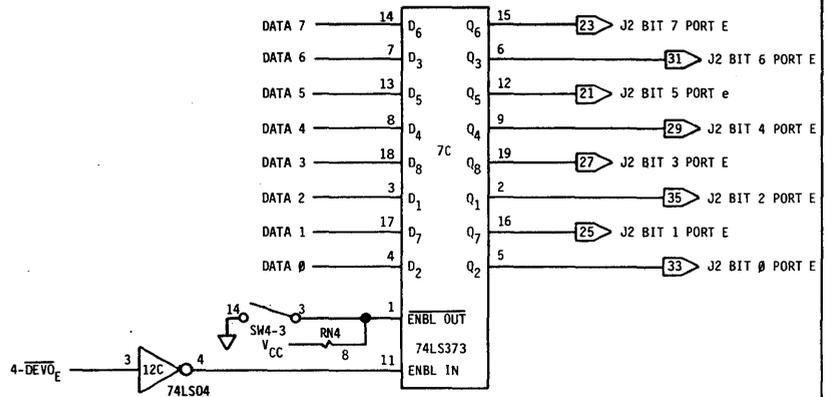
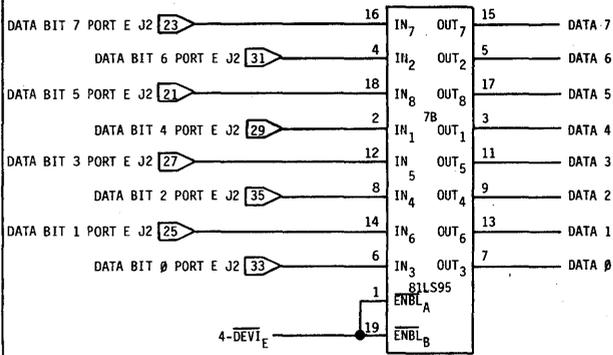
(pin # 1 is marked on the circuit board-- all odd pins are on the same row as pin # 1. The other row contains all even pins.)

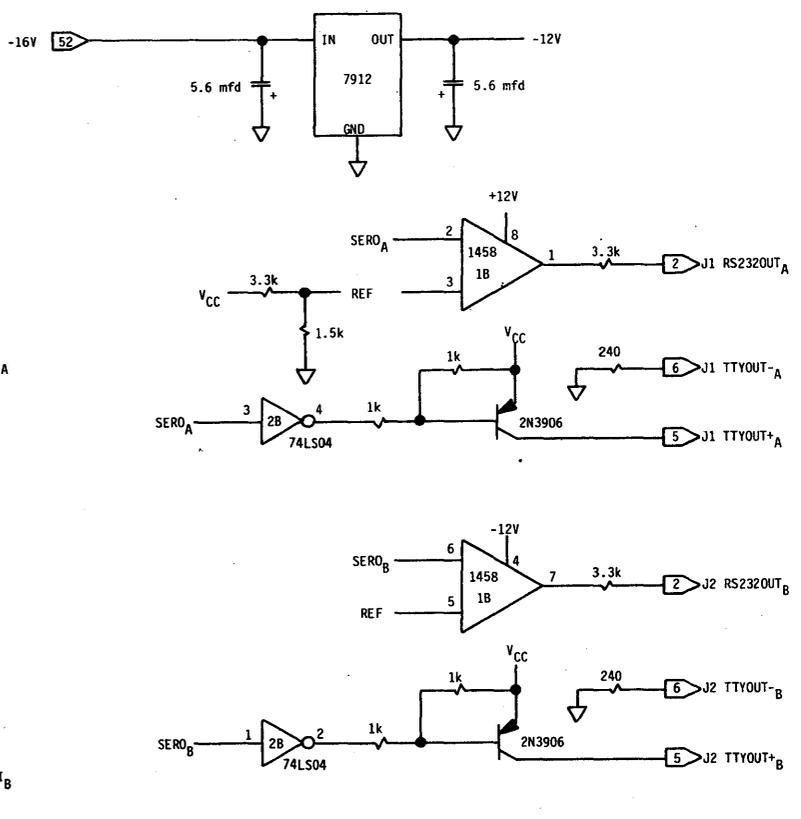
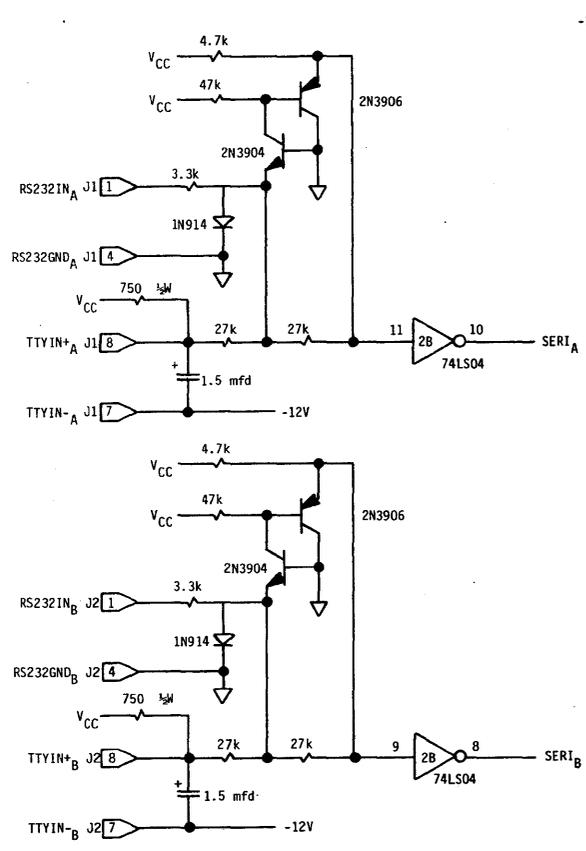
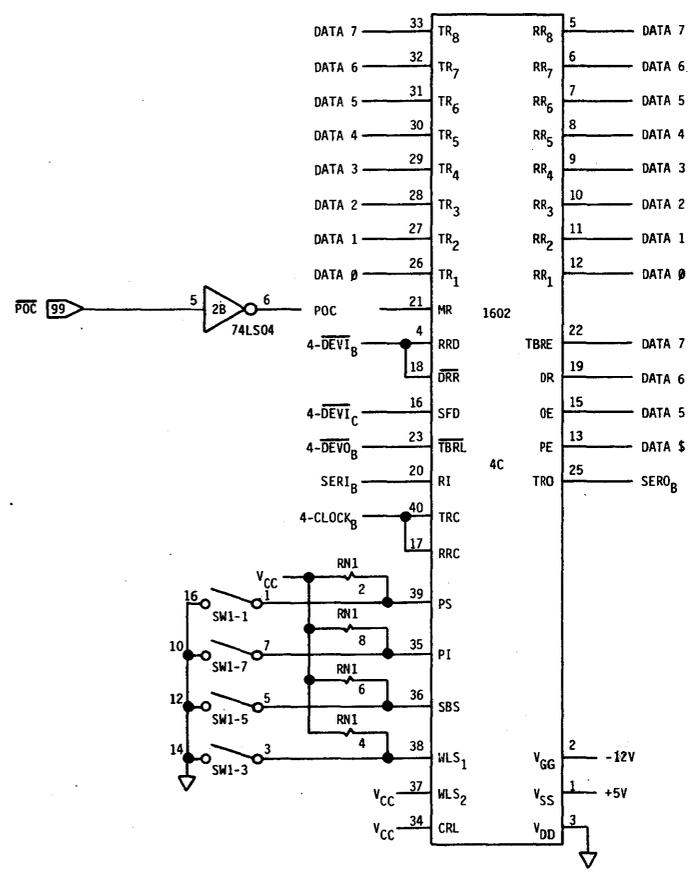
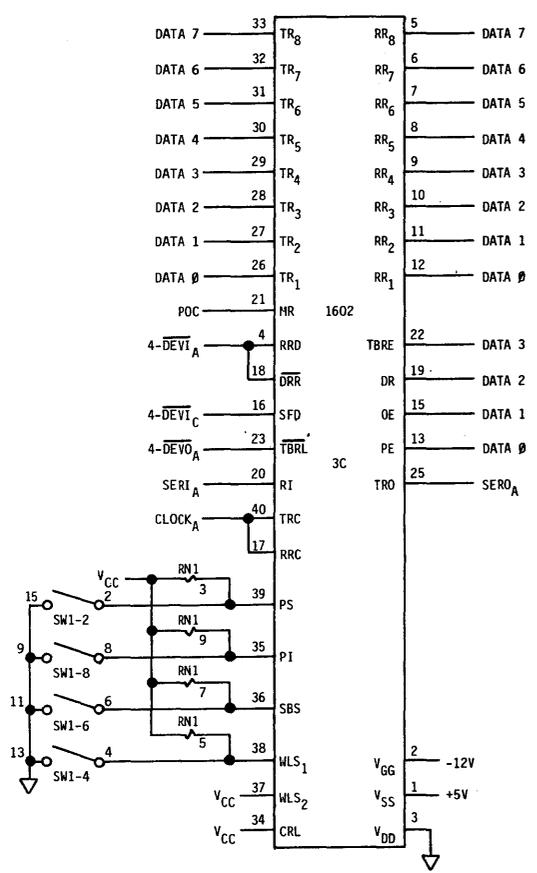












# Technical Data and Specifications

## SWITCHBOARD

### Compatible with the proposed IEEE S-100 Standard

#### Eight I/O Ports

8 I/O ports DIP switch selectable for location on any boundary of the I/O address space divisible by 8

#### Two RS232C/TTY current loop serial ports

- fully independent serial ports
- stop bit length selection
- parity enable selection
- parity even/parity odd selection
- seven or eight bit word length selection
- sixteen selectable baud rates from 50 to 19.2K

#### One serial status port

- serial port #1 — least significant 4 bits
- serial port #2 — most significant 4 bits
- receiver buffer full status
- transmitter buffer empty status
- parity error status
- over-run error status

#### Four Independent Parallel I/O Ports

Thirty-two lines of I/O available

Each group of eight lines DIP switch selected as input or latched output

Attention status bit for each group of eight I/O lines

#### Separate STATUS Port

One latched attention status bit for each parallel I/O port

Attention bit selected by DIP switch to latch on positive or negative pulse or level

Attention bit reset automatically by input reference of associated port

#### Separate STROBE Port

Eight independent strobe lines

Each line DIP switch selectable to be positive or negative strobe

#### Two 50-pin Flat Cable Connectors

One serial port, two parallel ports, two attention status bits, and four strobe lines per 50-pin connector

#### Power Requirements

5 volts @ 1 amp; 16 volts @ 150 ma; -16 volts @ 100 ma

#### 4K RAM Option

Eight 2114-3L 1Kx4 read/write static memory chips

Addressable by DIP switch on any 4K boundary

May be completely disabled via DIP switch so as to disappear from the address space of the CPU

#### 4K EPROM Option

Four 2708 1Kx8 eraseable programmable read only memory

Addressable by DIP switch on any 4K boundary

May be completely disabled via DIP switch so as to disappear from the address space of the CPU

#### Phantom Disable

DIP switch selection to allow the PHANTOM line to disable RAM and EPROM memory resident on the board

Specifications and prices subject to change without notice.

