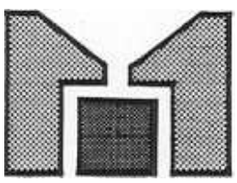
MACROTECH

V-RAM
Technical Manual



MACROTECH International Corp.
9551 Irondale Ave.
Chatsworth, CA 91311

MACROTECH V-RAM

MACRO-DRIVE/MEMORY

USER'S MANUAL

(Preliminary - July, 1985)

V-RAM MACRO-DRIVE/MEMORY BOARD

USER'S MANUAL

QUICK START

If you're interested only in getting the board up and running as fast as possible, skip to Appendix A.

MACROTECH International Corp.
818-700-1501

9551 Irondale Avenue
Chatsworth, CA 91331

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SECTION 1: INTRODUCTION

1 DUAL PURPOSE V-RAM

The Macrotech V-RAM Macro-Drive/Memory board offers two popular S-100 functions in a single product. To the host system, the board may appear either as a Macro-Drive (disk emulator) or system random access memory (RAM).

The V-RAM, by being completely self-contained, provides maximum reliability with minimum effort on the part of the user.

Accessed via S-100 ports, the V-RAM performs as a hardware disk simulator.

As a static RAM, the V-RAM exhibits the same speed and reliability as the Macrotech ST-Series RAM.

NOTE

The V-RAM board may be purchased strictly as a 256 kilobyte, non-volatile static RAM. In this configuration, none of the disk emulation functions are available.

1.2 MACRO- DRIVE (DISK EMULATOR)

1.2.1 Dual Capability

Purchase of a disk emulator represents considerable investment of funds for most customers, as does the acquisition of additional system memory. Other disk emulators perform only the function of "disk emulation". Expansion of system memory requires additional expenditure for a memory board.

The V-RAM addresses this problem by performing equally well in either or both tasks.

1.2.2 Use of Currently Available Software

The Macro-Drive may be driven by any software presently configured for CompuPro's M-Drive/H board. Up to 8 units are "cascadeable" as in the M-Drive/H.

In addition, the unit may be accessed as normal system memory if so enabled upon installation. The base address of the board may be set to any 64K byte boundary within the S-100's extended addressing range of 16 megabytes independently of the unit's port address setting for the purposes of disk emulation.

One interesting possibility arises from this arrangement. A program debugger may be used to "examine" the contents of disk files which have been copied to Macro-Drive (the disk emulator function of the V-RAM) and if desired, files may be altered or patched and then re-written back to a physical disk. This capability may be very useful to those performing development work.

NOTE

> Depending on the software which is accessing the V-RAM as a disk emulator, a "checksum" or "parity" byte may also require updating whenever data is altered in the V-RAM "sector" prior to accessing this data as a "disk" file. Refer to Appendix B.

1.2.3 High Speed Memory

The fastest-possible disk emulator in terms of memory speed and cycle time is ensured by the use of static RAM on the Macro-Drive.

1.2.4 Fail-Safe Operation

A potentially serious problem arises from the use of volatile RAM for storing disk files. Power outages or even "kicking the power cord" could cause catastrophic loss of file data in the disk emulator. This is not a problem with the non-volatile V-RAM.

CMOS static RAM makes self-contained battery backup feasible. Macrotech's implementation of this feature makes it "hassle-free" for the user, in that no special wires need be routed to the V-RAM, nor do any S-100 pins need re-defining as with some system battery backup schemes.

Power fail detection and memory data protection for a 7-week minimum are completely self- contained on the Macro-Drive board.

With proper support software, a system may be made completly "fail- safe" as far as power outages are concerned. Another possibility for taking full advantage of the non-volatile nature of the V-RAM as system memory is to leave the operating system loaded on the board. Each time the system is powered-up, a simple jump is performed to the "cold-boot" entry point of the operating system, thus booting the system without waiting for any disk read operations.

STATIC CMOS MEMORY

1.3.1 Major Features

The V-RAM board incorporates full power and ground planes for electrically quiet, reliable operation. Major features of the memory array include:

a. Maximum density of 512 kilobytes in a single S-100 bus slot is achieved through careful layout and use of host/adapter board expansion architecture.

b. 8/16-bit data transfer protocol is supported in full compliance with the IEEE/696 standard.

c. Chip select on address assures the fastest access time possible. Every S-100 CPU board available today presents valid addresses to the bus earlier than either control or data strobes. The V-RAM achieves faster access time by starting memory cycles at the moment addresses are valid.

1.3.2 MEMORY LOSS PROTECTION

The battery backup feature available to the Macro-Drive may also be used in System Memory applications. When data integrity must be maintained, even during brownouts or AC line failures, correct implementation of the S-100 PWRFAIL* signal is essential.

Typical standby power consumption for a fully populated memory array is less than 0.064 milliamps at 2.2 volts. This means that the small, 110 milliamp-hour backup battery is able to maintain data for 1,720 hours (71 days or 10 weeks).

Modern Ni-Cd batteries, particularly the one chosen for this application, no longer suffer from the "memory" phenomenon which plagued earlier Nickel-Cadmium cells.

For those who are not familiar with this problem in Ni-Cd cells, the term "memory" in relation to Ni-Cd technology has nothing to do with storing computer data.

It refers to the fact that earlier cells with a given capacity rating, when used repeatedly to supply less than their full capacity, slowly became unable to deliver their rated power. In effect they "remembered" their previous discharge level.

Thus if the V-RAM, utilizing "old" type Ni-Cd cells, were rated for a minimum data retention of 10 weeks, and the user had turned his machine off for only 18 hours each night for 100 nights, he might then go on vacation for 1 week and find that data had been lost because the Ni-Cd battery "remembered" supplying 18 hours'-worth of power.

Again, this is NOT a problem with today's Ni-Cd cells.

1.3.3 Low Power Consumption

A fully populated V-RAM, when active, consumes less than 870 milliamps (850 ma typical). When configured with 256 kilobytes of RAM, this figure drops to less than 820 milliamps with a typical current draw of 810 milliamps.

The RAM IC's chosen for the V-RAM are "Low Power" versions of the popular 8K X 8 fully static CMOS RAMs. This guarantees that during power-down mode (standby) that each RAM IC draws less than one-millionth of one amp (1 microamp) from the backup battery.

1.4 BOARD ELEMENTS

The Macro-Drive/Memory board consists of 512 kilobytes of CMOS static RAM and a RAM controller circuit. Circuit components are aranged on a 5-layer host printed circuit (PC) board and a 4-layer adapter board. Included on the host board are four sets of resettable box jumpers or "switches" to allow complete flexibility in reconfiguring the board for various addressing modes.

A battery charging circuit of the constant current type is provided. Battery isolation during power on is provided by a current limiter Q2 (LM334) in the path of V+ to the RAM array, which blocks up to 40 volts in the reverse direction. During power down, the on-board battery is prevented from supplying current to the rest of the system by the blocking action of the diode D6 (when jumper J17 is installed).

If need be, an open-collector transistor driver is provided to drive one of the following bus lines:

a. WAIT*

b. PWRFAIL* (13)

c. NMI*

whenever the V-RAM's internal logic detects that the unregulated +8 volt line is too low to provide reliable operation of the board.

1.5 SPECIFICATIONS

Specifications of the V-RAM are summarized in Table 1-1

	V-RAM Specifications
PC Card	Full power and Ground planes. 5-layer host; 4-layer adapter.
Speed	10 nanoseconds access (typ), processor-dependent, measured from leading edge of pSTVAL. 155 nanoseconds from address valid.
Size	512 kilobytes, 256 kilobytes.
Addressing	Base-addressable on any 64K Boundary within the S-100 IEEE/696 specified 16 megabyte extended (24 bit) address range.
Data Width	8 or 16-bit (byte or word).
Dimensions	Overall physical size in accordance with IEEE-696. Full 512K Host/Adapter pair is less than 0.720 in thickness, allowing installation in most S-100 chassis without skipping slots.
Power Requirements	Less than 1.0 amps (850 milliamps typical) from the unregulated 8-volt lines (S-100 pins 1 and 51).
Battery Requirements	Fully self-contained battery and charger circuit retains data for at least 10 weeks. External battery may be used via S-100 pin 21 at 2.2 to 2.4 volts, less than 64 microamps (0.000064 Amps) current per V-RAM board. (A typical "C" cell would hold data for nearly 2 years.)
Warranty	All MACROTECH products carry a FULL ONE-YEAR factory warranty.

Table 1-1.

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SECTION 2: CONFIGURING V-RAM

2.1 FACTORY SET-UP

As shipped from the factory, the V-RAM is set to emulate a disk drive in any standard "CompuPro-style" environment, as 512K disk emulator board #0. The System Memory portion is DISABLED. Refer to table 2-1.

FACTORY CONFIGURATION SETTINGS

JUMPER	SETTING	FUNCTION	CONDITION	
J1	Right	Board Number B0	0	Disk Emulator
J2	Right	Board Number B1	0	portion of board
J3	Right	Board Number B2	0	set as board #0
J4	Left	Base Address A23	0	System Memory
J5	Left	Base Address A22	0	portion of board
J6	Left	Base Address A21	0	begins at address
J7	Left	Base Address A20	0	070000H
J8	Left	Base Address A19	0	
J9	Right	Base Address A18	1	
J10	Right	Base Address A17	1	
J11	Right	Base Address A16	1	
J12	Left	Memory Function	Disabled	
J13	Right	Disk Emulator	Enabled	
J14	Left	Phant* Pullup	Connected to bus	
J15	Right	Phant* Recognition	Enabled	
J16	Left	Sxtrq* Pullup	Connected to bus	
J17	Up	External Battery	Disconnected from bus	
J18	Down	Port Address A1	1	Disk Emulator
J19	Down	Port Address A2	1	portion of board
J20	Up	Port Address A3	0	has Port Base
J21	Up	Port Address A4	0	Address of 0C6H
J22	Up	Port Address A5	0	
J23	Down	Port Address A6	1	
J24	Down	Port Address A7	1	
J25	Missing	Bus Power Failure	Not driving any S-100 signal lines	

Table 2-1

2.2 REQUIRED OPERATING SYSTEMS

In order to take advantage of existing Disk Emulator support software, most operating systems purchased from CompuPro will support this type of hardware. Here is a list of Operating Systems and revision levels which already include the correct BIOS support:

(operating systems purchased from CompuPro, where the revision number is equal to or greater than...)

a. CP/M 80: CP/M 2.2MDB or higher.
b. CP/M 86: CP/M 86 1.1NAA or higher.
c. MP/M 816: MP/M 816 2.1D or higher.

2.3 RECONFIGURING THE V-RAM

2.3.1 Procedure

If your disk system was not supplied by CompuPro, but uses a standard version of CP/M 2.2, or if you have an older version of a CompuPro-style operating system, you may elect to enhance your operating system BIOS (see Appendix C), or write a small program to take advantage of the V-RAM feature.

The following steps are recommended (refer to Appendix A for explanation of each switch and its function) :

a. Set port base addresses to an UNUSED port in your system.

b. Set Board Number in switches J1, J2, and J3 (if only one V-RAM or M-Drive/H is in the system, it MUST be set to 0. A second board must be set as #1, a third as #2 etc.)

c. If you desire the board to function as a System Memory IN ADDITION to functioning as a Disk Emulator;

   1. Set the Memory Base Address for the desired starting address of the board (usually the next higher address above existing system memory).

   2. Enable the System Memory function and the Disk Emulator function by placing J12 and J13 to the right (respectively).

NOTE

Be careful when setting the Base Address of the board. A potential exists for loss of data if the V-RAM portion of System Memory is written-to which happens to overwrite a "Disk" file, or the Disk Emulator is written to which overwrites System Memory data. For this reason, both functions may NOT be used together if the board's Base Address is set to 0000 (with any operating system that loads to low memory).

d. If you desire to use the V-RAM as System Memory only, you need only follow step (c.) above with the exception of moving J13 to the left, DISABLING the Disk Emulator function.

e. Install the V-RAM board as indicated in the last part of this section.

2.3.2 Setting Port Addresses Jumpers

Jumper switches J18 through J24 are used to select the base port addresses (usually C6 Hex) for the Macro-Drive function.

NOTE: "0" = ON (Jumper set up). "1" = OFF (Jumper set down)

2.3.3 Set Cascade Address (Disk Emulate Board Number)

Jumpers J1, J2 and J3 on the board are used to select the Macro-Drive cascade address. To set the address:

a. First, determine how many V-RAM boards are to be used in the system.

b. Each V-RAM or M-drive/H must have its own Cascade Address (0 through 7).

c. Set the jumpers on each board as follows:

Disk Emulator Board Number		J3	J2	J1
FIRST	(0)	Right	Right	Right
SECOND	(1)	Right	Right	Left
THIRD	(2)	Right	Left	Right
FOURTH	(3)	Right	Left	Left
FIFTH	(4)	Left	Right	Right
SIXTH	(5)	Left	Right	Left
SEVENTH	(6)	Left	Left	Right
EIGHTH	(7)	Left	Left	Left

2.3.4 Set System Memory Base Address

Jumpers J4 through J11 on the board are used to select the Base Address if the V-RAM is to be used as a System Memory. To set the address:

a. First, determine the desired starting address. This must be 0 (low memory) or a number divisable by 64 (e.g. 64K, 256K, 512K, 2048K (2 Meg)).

b. Divide this number by 64 to obtain the "bank number".

c. Set the switches J4 through J11 to the binary number representing this "bank number", J4 is the Most Significant Bit (MSB) and J11 is the Least Significant Bit (LSB). 0's are represented by installing the jumper in the Left position, and 1's by installing the jumper to the Right.

   See Appendix D for table of all possible Base Address settings.

Another way to consider this is to set the Jumper Switches to "match" the desired starting address on the bus. J4 through J11 must "match" A23 through A16 respectively to define the first (lowest) System Memory address on the V-RAM board. See Appendix D

INSTALLING THE BOARD

a. Power-Off Check

CAUTION - Before removing or installing any boards in the host system, make sure power is turned off to the system.

b. Install Board

Plug the V- RAM into the system chassis

c. Turn on system power

d. Perform "BOOT"

Boot as you normally would, (i.e. Insert a floppy diskette into drive (A) or allow the hard disk to perform a normal "boot"). If you have an appropriate operating system as outlined in section 2.2, then at this time, the Macro-Drive is automatically formatted for use and the operating system will inform you of how may Kilobytes of M-DRIVE are active in the system. If the size seems incorrect, power down the system and check the switch settings on each board.

e. Use the V-RAM as you normally would any disk drive (PIP files to/from it, log onto the drive, run assemblies or compile operations with great speed.

2.5 USING THE MACRO-DRIVE

2.5.1 READY FOR USE AFTER FORMATTING

Once the Macro-Drive is formatted, it is ready for use. Treat it as you would any other floppy disk drive in your system. For example, you may PIP files to it, run programs from it or use STAT to find out how big it is. You will notice that operations will be executed MUCH faster on the Macro-Drive.

2.5.2 Reformatting

At any time, you may "force" a reformat of the drive through use of the MFORM command. Just:

a. Type in MFORM M.

b. Press the Carriage Return Key.

c. The program will ask you if you really want to reformat the Macro-Drive.

d. Enter Y for yes (if you wish to reformat the Disk Emulator)

NOTE

If you wish to reformat, remember that the files previously on the Disk Emulator will be erased.

e. The Disk Emulator function of the V-RAM is now "clean" and drive (M) is ready to accept new files.

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SECTION 3: BACKUP POWER SOURCE SETUP

3.1 BACKUP POWER DISCUSSION

The V-RAM uses low power CMOS RAM chips, plus a separate power plane on the printed circuit board for those chips, to permit independent application of power from a backup battery source in case of failure of normal system power.

V-RAM contains its own circuitry for providing Battery, Battery-charger, Backup Voltage Regulation, and Power Fail Detection, on the V-RAM board itself. NO EXTERNAL LOGIC OR BACKUP POWER SOURCE IS NORMALLY REQUIRED.

However, if for some reason you desire to utilize external backup battery, this outlines the requirements for doing so:

Bus pin 21 is listed in the IEEE/696 standard as "undefined". In Macrotech systems, this bus line carries backup battery power to the CMOS RAM.

Pin 21 is the board's battery power source when jumper J17 is installed in the bottom position. If J17 is omitted or set up, the board will function normally, but backup power will be sourced from the on-board Ni-Cd battery.

Power for the RAM chips in "standby" mode will come from the external battery whenever J17 is in the down position, and the voltage on pin 21 remains between +2.4 and +4.0 volts.

NOTE

The V-RAM's battery charges at a fixed rate of 10 milliamps whenever system power is applied. When system power is OFF, this power is used from the cell at a current drain of approximately 64 microamps. This means that once the Ni-Cd battery on the V-RAM is charged to a nominal 2.6V open-circuit voltage, 1 hour of charging (system power ON) is required for every 150 hours of battery back-up time.

BACKUP MODE OPERATION

The battery backup mode is invoked if the V-RAM's analog circuitry detects that the unregulated +8 volt line (S-100 pins 1 and 51) is too low to reliably sustain a VCC of +5V to the other on-board logic (this normally is when the +8V line drops to approximately 7.4 volts). The V-RAM then disables its write enable and chip select logic and blocks all spurious memory accesses until the detection logic determines that normal power has been restored.

The V-RAM's battery charges at a fixed rate of 10 milliamps whenever system power is applied. When system power is OFF, this power is used from the cell at a current drain of less than 64 microamps. This means that once the Ni-Cd battery on the V-RAM is charged to a nominal 2.6V open-circuit voltage, 1 hour of charging (system power ON) is required for every 150 hours of battery back-up time.

As an additional feature, the V-RAM includes an open-collector driver (transistor) conforming to IEEE/696 specifications which may be connected to the bus via J25, a 4-pin jumper (unmarked) located between resistors R5 and R7, just above and to the right of the upper-end of the battery.

Installing a jumper shunt at J25 from the center pin to one of the other three pins will drive one of three S-100 signals as follows:

J25 installed center pin to	drives S-100 signal (pin) with open-collector	
Up	NMI*	(12)
Right	PWRFAIL*	(13)
Down	WAIT*	(72)

The V-RAM will be in low-power standby mode until the unregulated +8 volt line returns to a nominal level. This mode is particularly useful for virtual disk applications, since it assures the continued integrity of the contents of the virtual disk after either loss of power or a normal system shutdown.

3.3 BACKUP POWER REQUIREMENT

To use the V-RAM's battery backup mode successfully, your system must have a backup power source (battery) capable of providing at least 100 microamps at 2.4 volts to each V-RAM board for the entire backup period. The power source must be connected to bus pin 21 (termination should be removed if present on this line) and the V-RAM switch J17 should be installed in the down position.

If bus pin 21 is already used by other boards in your system for some other purpose, you will have to use on of the other NDEF lines (65 or 66) for the Vbat battery backup line. J17 must be disconnected. Its center pin must be patched to the chosen NDEF bus pin.

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SECTION 4: EASY FIXES TO COMMON IEEE/696 DEVIATIONS

4.1 FLOATING LINES

Certain older systems had no provision for some of the lines defined in IEEE/696 and used by Macrotech memory. Whether or not they are driven, these lines must be pulled up high with resistors for the system to work reliably. The V-RAM provides pullup resistors, jumper-selectable, for PHANT* AND SXTRQ*.

JUMPER	FACTORY SETTING	FUNCTION	CONDITION
J14	Left	Phant* Pullup	Connected to bus
	Right	Phant* Recognition	Enabled
	Left	Sxtrq* Pullup	Connected to bus

J14 is not required if (1) Phantom* is not used by your system - or - (2) a pullup is provided elsewhere in the system.

In some user systems, the bus terminator network has pullups to pull these lines high, even if no board in the system will drive them low. In other systems, more than one board may provide pullups for these lines (more than one Macrotech board, for instance). No more than one pullup should be enabled for each of these lines, in order that their open-collector drivers won't have to sink excess current. If there is any doubt about this, however, it is best to use the onboard pullups, to ensure that bus noise on these lines can't cause erratic behavior.

4.2 POWER-OK IN ALPHA MICRO SYSTEMS

ALPHA MICRO 100L: The PWRFAIL* signal at bus pin 13 is reversed in function. It goes low, not high, when system power is okay. The AM100L is not listed as IEEE/696, so this is not illegal, but this will lock up the system if J25 is installed to drive pin 13.

SECTION 5: JUMPER SETTINGS SUMMARY

5.1 HOST BOARD JUMPERS

5.1.1 Selectable Options

The resettable box jumpers or "switches" on the V-RAM host board allow complete flexibility in reconfiguring the V-RAM for your particular needs. The circuitry is switch-selectable for:

a. Desired function (disk emulator and/or system memory).

b. Port address (for disk emulate function only).

c. Disk emulation unit selection.

d. RAM base address.

Setting circuit parameters for each of these functions is covered in the following subsections.

5.1.2 Default Settings

Factory settings of the jumpers are shown in Table 2-1. These settings configure the V-RAM for direct replacement of the CompuPro M-Drive/H board for disk emulation. For an explanation of what these settings provide, refer to the jumper summary tables in Appendix A.

5.1.3 Reconfiguration Procedure

NOTE

You don't have to remove the adapter board to get at the jumpers on the host board.

a. First, read the material in the summary tables and decide how to position the jumpers. If necessary, review the corresponding writeups in Sections 2 through 4.

b. Set the switches as desired.

c. Make a power-off check of the system. (Make sure power is turned off to the host system.)

d. Install the board in any slot in the system chassis.

FUNCTION ENABLE

It is possible to set the V-RAM to perform disk emulation, system memory or both functions. Corresponding switch settings are specified in Table 5-1.

JUMPER	SETTING	FUNCTION	CONDITION
J12	Left	Memory Function	Disabled
J12	Right	Memory Function	Enabled
J13	Left	Disk Emulator	Disabled
J13	Right	Disk Emulator	Enabled

Table 5-1. Function Enable Settings

5.3 PORT ADDRESS

When running the V-RAM in Macro-Drive mode, the board requires two consecutive port addresses. The first or "Base Address" is set up in the jumper switches J18 through J24. The second port Address is recognized automatically as (Base Address +1).

Seven jumper switches are used to set a pattern to match the upper 7 bits of the port address during disk emulation operations (refer to Appendix A). J24 through J18 represent A7 through A1, respectively. A jumper installed down represents a "1" in the port address. A jumper installed in the up position represents a "0". Refer to Table 2-1 for the "normal" factory settings which are required for most M-Drive support software.

J24	J23	J22	J21	J20	J19	J18	PORT ADDRESSES
Up	Up	Up	Up	Up	Up	Up	00 and 01
Up	Up	Up	Up	Up	Up	Down	02 and 03
Up	Up	Up	Up	Up	Down	Up	04 and 05
Up	Up	Up	Up	Up	Down	Down	06 and 07
Up	Up	Up	Up	Down	Up	Up	08 and 09
Down	Down	Down	Down	Up	Up	Up	F0 and F1
Down	Down	Down	Down	Up	Up	Down	F2 and F3
etc.							

Table 5-2. Port Address Settings

5.4 DISK EMULATION UNIT SELECT

Up to 8 V-RAM's may be used in a system. A cascade (unit select) address must be established for each board set up for disk emulation (Macro-Drive).

The first such V-RAM or M-Drive/H in each system must be set as unit "0". Each additional V-RAM or M-Drive/H must be set to the next higher unit number (i.e. 3 units in the system must be set as units 0, 1 and 2). The unit number (0 through 7) is set by jumper switches J1, J2 and J3. Refer to section 2.3.3.(c.) for a complete listing.

This "cascade address" is not to be confused with the Port Address discussed in section 5.3.

5.5 RAM BASE ADDRESS

When accessing the V-RAM as system memory, the base address of the board may be set to any 64K boundary within the 24-bit S-100 extended range.

Jumper switches J4 through J11 are used for this purpose (refer to Table 5-4).

To set the switches properly, take the desired starting address of the board (the base address must be a multiple of 64K) and divide it by 64. The resultant number is the "bank number".

Set jumper switches J4 through J11 to the bank number, where J4 is the most significant bit and J11 is the least significant bit. Setting any of these jumper switches to the left represents a "0"; setting a switch to the right represents a "1".

Refer to examples in Table 5-4.

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SECTION 6: FUNCTIONAL DESCRIPTION

6.1 DISK EMULATION

6.1.1 Accessing Disk Files

Your computer's operating system accesses disk files through a set of "driver routines", which handle such tasks as seeking a desired disk track, selecting a desired read/write head and actually transferring data to or from a desired sector of the disk or diskette. Thus, the operating system itself has no knowledge of the physical nature of the disk drive in use. Any device which is able to store and retrieve data, where the driver routines transfer such data in blocks logically defined as "sectors" which in turn comprise "tracks", may function as a disk drive. In an actual disk drive, delays are incurred at three points in the read or write operation:

a. Positioning the read/write head to the desired track.

b. Waiting for the disk or diskette to turn (spin) until the desired sector is in place beneath the read/write coils.

c. Moving the data to or from the media (disk) and the desired data location in memory.

6.1.2 Read/Write Times

Table 6-1 below compares the time required for reading 128 bytes from a standard 8-inch "floppy" diskette using a typical Winchester (ST-506 standard) and Macro-Drive. (It is assumed the floppy drive has a single-density IBM format and a 15 ms step rate.) Whole figures are rounded off to the nearest millisecond.

Type Of Operation	Floppy Mean Time	Floppy Worst Case	Winchester Avg. Time	Using Macro-Drive
Seek Track	570 ms	1140 ms	45 ms	0 ms
Seek Sector	83 ms	167 ms	8 ms	0 ms
Transfer Data*	4 ms	4 ms	0.338 ms	0.338 ms (8 MHz Z80)
Total Time	657 ms	1311 ms	53 ms	0.338 ms

* Winchester "transfer date" time of 0.205 milliseconds, if full DMA.

Table 6-1. Floppy Diskette And Macro-Drive Read/Write Times

6.1.3 Macro-Drive Advantage

As you can see, considering disk read/write operations only, the Macro-Drive has a potential average advantage of 194,300 percent over a single-density floppy and a more pedestrian 15,600 percent (156 times faster) speed advantage over standard Winchester drives.

Of course, the speed with which data is moved to and from the disk has a varying effect on the overall execution time of a program. Using Macro-Drive yields the greatest performance increase in the execution of assemblers, compilers and data-base management programs where disk use is intensive. It would be reasonable to expect that an assembly job which previously consumes 6 minutes may run in less than 1 minute with Macro-Drive.

6.2 V-RAM DATA TRANSFERS

The V-RAM looks like two input/output ports to the system bus. One I/O port is used to load a starting address into the board.The other port is for reading data from or writing data into the RAM.

The starting address is loaded into a 24-bit counter on the board by performing 3 consecutive port writes (out's) to port #(Port Base Address +1). Data is then read or written by performing port reads or writes (in's or out's) to port #(Port Base Address).

After each data access (read or write), the address counter automatically INCREMENTS, pointing to the next byte address without requiring a new value to be written to the counter.

Each V-RAM board must be accessed as one of eight possible V-RAM's or M-Drive/H's in the system. Board selection is the simple result of the counter exceeding 512K of ram space and the upper bits of the counter forming a 1 of 8 select as follows:

a. All Disk Emulator boards in the system share the SAME PORT ADDRESS. Therefore, at the time of address initialization, (refer to the discussion above), ALL disk Emulator boards in the system HAVE THE SAME ADDRESS.

b. All Disk Emulator boards in the system auto-increment TOGETHER, regardless of the condition of Board Select, whenever data is input or output through the data port address (Port Base Address). Again, ALL Disk Emulator boards inthe system have THE SAME ADDRESS in their respective counters.

c. The settings of J1, J2, and J3 form a 3-bit compare value which is compared directly to address bits 19, 20, and 21 (respectively) of the 24-bit counter which maintains the Disk Emulator Address (not to be confused with any S-100 address bits).

d. Therefore, as the counters on all boards increment together past the 512K capacity of the first Disk Emulator board in the system (Board Select number = 0), all counters begin to assert bit 19 high.

e. The first board no longer has a true compare (e.g. J1, J2, and J3 all set to "0" is NOT EQUAL to the upper counter bitrs where B19 = 1, B20 = 0, B21 = 0).

f. The SECOND board in the system should now have a TRUE compare since J1 is set LEFT ("1"), J2 Right ("0"), and J3 Right ("0").

g. After another 512K, counter bit 19 will be "0" again but bit 20 will go to "1", where the third board (board number 2) takes over; etc...

RAM ADDRESSING

When the V-RAM is accessed as normal system memory, address bits A0 through A18 are buffered through the 74LS244s at locations F3, F6 and F8 to become the terms AB0 through AB18. The address bits A19 through A23 are not beffered in this manner, because each of these lines is used at only one input on the V-RAM.

Any access of the RAM (reading or writing) must "select" one or two 8K X 8 CMOS RAM devices, depending on whether the access is an 8- or a 16-bit transfer. Each RAM device has two select terms for this purpose. All RAM devices belong to one of two groups, designated even or odd. All even RAM devices have their high-active select term true during eighter a 16-bit access or an 8-bit access, where @-100 address bit A0 is low. All odd RAM devices have their high-active select terms true during either a 16-bit access or an 8-bit access where S-100 address bit A0 is high.

The second select term of each RAM devicer is a low-active term designated "chip select". The RAM devices on the V-RAM board are organized so that during any RAM access, only one of 32 signals (designated CS0* through CS31*) is active during any one cycle. (A 256 kilobyte V-RAM board has only 16 "chip select" lines.)

The terms CS0* through CS31* are output by one of four 74LS138s at location C4 and C5 on the host board and locations K5 and K6 on the adapter board. This array of 74LS138 selectors obtains its binary-encoded input through the data selectors (74LS157s) at locations D4 and D5 and directly from the buffered address lines AB14, AB15 and AB16. The data selectors drive the CS* selectors from one of two sources, depending on whether the present operation is disk emulation or system memory.

In the case of system memory access, the summed portion of the binary-encoded Chip Select number is gated through the data selectors from the 8-bit full adder comprised of the 74LS253s at locations E4 and E5. The least significant bit of the sum is ignored, and the remaining value must represent a number between 0 and 3 in order for the board to be selected.

In greater detail:

a. Address terms AB16, AB17 and AB18 (along with A19 through A23) form an 8-bit augend to the adder.

b. Jumper-switch settings J4 through J11 form the addend.

c. Since the switches J4 through J11 are set to the complementary signal (i.e., a "0" bit is represented by +5 V and a "1" bit is represented by ground potential), the addend is actually the "ones-complement" of the desired bank number.

d. The "carry-in" bit of the 8-bit adder is tied to +5V, thereby always adding 1 to the "ones-complement" addend, which makes it a "twos-complement" number.

e. In binary arithmetic, addition of a number's "twos complement" has the effect of subtracting that number from the augend. Thus, we have "subtracted" the desired bank number for the board's base address from the physical address being presented on the S-100.

f. This assures that when the S-100 bus address equals the desired bank number (64K boundary) for the base address of the board, the output of the 8-bit adder always equals "00'. As the S-100 address increments to 128K above the bse address, the output of the adder is "01", and so forth.

g. When the S-100 address exceeds 512K above the base address of the board (or 256K above in the case of a 256K configured V-RAM), one or more of the sum bits from the adder going high tell the PAL at location D6 that this board is no longer selected, and the terms BDSEL* and ADDR* are no longer true during a cycle. This inhibits the PAL at location C6 from gating the data buffers (74LS245s) at locations F9, F11 and F12 onto the S-100 bus.

PORT ADDRESSING

NOTE

Access to the V-RAM via port input and outputs is not possible in the 256 kilobyte configuration. Most of the necessary hardware is installed on the adapter board (the board containing the second 256 kilobytes of RAM).

When the V-RAM is accessed as a disk emultor, the presence of the proper port address is detected via an 8-bit match-detector, the 74LS521 at location F6. The jumper-switch setting on J18 through J24 for the port address select is compared directly with the seven address bits A1 through A7 from the S-100 bus.

The proper S-100 status sOUT or sINP is decoded in the 74LS32 at location C2 and this signal qualifies the "match" detected at the IC location F6.

6.5 LOADING THE DISK EMULATOR RAM ADDRESSES

Writing to the control port address causes data to be latched into the 74LS461 octal counters at locations L6, L8 and L10 on the adapter board. The physical location of these devices on the board is what precludes the use of the V-RAM as a disk emulator in its 256K configuration.

Data latched into the first counter on a control port write is presented to the data inputs of the second counter on the next write, and so on to the third and last counter in the series. Thus, if it weere desired to write the 22-bit address 123456H into the entire latch, one would first output the value 12H followed by 34H and finally 56H to the control port address.

6.6 BATTERY BACKUP

The self-contained battery backup consists mainly of a power cell, two voltage comparators and a regulator to control power to the RAM devices in the power-down mode.

When one of the voltae comparators detect that the Vcc to the RAM devices has fallen below an acceptable value (i.e., the last moment during power failure that reliable operation of the RAM can be assured), it causes the VOK* signal to go false, thus forcing a de-select of all RAM devices, regardless of the current operation on the S-100 bus. This does not cause any external signal which may be used by the S-100 bus.

It is anticipated that another board in the system will support "imminent power failure" logic, which may signal the CPU early enough to allow it to perform "housekeeping" prior to system failure.

Some time after the RAMs have been disabled by this logic, the regulated Vcc to the RAM array will fall lower than a nominal 2.2 volts, at which time the backup battery will be the source of current (approximately 90 milliamps) to the RAM devices through the LM334 current limiter, ensuring the integrity of all data stored there.

Appendix A - QUICK SET-UP AND SWITCH DEFINITIONS

SETTING FOR USING AS DISK EMULATOR ONLY (BOARD #0)
IN STANDARD M-DRIVE/H ENVIRONMENT (i.e. CompuPro software

JUMPER	SETTING	FUNCTION	CONDITION	
J1	Right	Board Number B0	0	Disk Emulator
J2	Right	Board Number B1	0	portion of board
J3	Right	Board Number B2	0	set as board #0
J4	XX	Base Address A23	X	System Memory
J5	XX	Base Address A22	X	Base Address is
J6	XX	Base Address A21	X	a "don't care"
J7	XX	Base Address A20	X	
J8	XX	Base Address A19	X	
J9	XX	Base Address A18	X	
J10	XX	Base Address A17	X	
J11	XX	Base Address A16	X	
J12	Left	Memory Function	Disabled	
J13	Right	Disk Emulator	Enabled	
J14	XX	Phant* Pullup	"Don't care"	
J15	XX	Phant* Recognition	"Don't care"	
J16	XX	Sxtrq* Pullup	"Don't care"	
J17	Up	External Battery	Disconnected from bus	
J18	Down	Port Address A1	1	Disk Emulator
J19	Down	Port Address A2	1	portion of board
J20	Up	Port Address A3	0	has Port Base
J21	Up	Port Address A4	0	Address of 0C6H
J22	Up	Port Address A5	0	
J23	Down	Port Address A6	1	
J24	Down	Port Address A7	1	
J25	Missing	Bus Power Failure	Not driving any S-100 signal lines	

SETTING FOR USING AS SYSTEM MEMORY ONLY

JUMPER	SETTING	FUNCTION	CONDITION	
J1	XX	Board Number B0	0	"Don't care"
J2	XX	Board Number B1	0	"Don't care"
J3	XX	Board Number B2	0	"Don't care"
J4	Left	Base Address A23	0	System Memory
J5	Left	Base Address A22	0	portion of board
J6	Left	Base Address A21	0	begins at address
J7	Left	Base Address A20	0	000000H
J8	Left	Base Address A19	0	- See Appendix D
J9	Left	Base Address A18	0	for fullo listing
J10	Left	Base Address A17	0	of all possible
J11	Left	Base Address A16	0	address settings
J12	Right	Memory Function	Enabled	
J13	Left	Disk Emulator	Disabled	
J14	Left	Phant* Pullup	Connected to bus	
J15	Right	Phant* Recognition	Enabled	
J16	Left	Sxtrq* Pullup	Connected to bus	
J17	Up	External Battery	Disconnected from bus	
J18	XX	Port Address A1	X	"Don't care"
J19	XX	Port Address A2	X	"Don't care"
J20	XX	Port Address A3	X	"Don't care"
J21	XX	Port Address A4	X	"Don't care"
J22	XX	Port Address A5	X	"Don't care"
J23	XX	Port Address A6	X	"Don't care"
J24	XX	Port Address A7	X	"Don't care"
J25	Missing	Bus Power Failure	Not driving any S-100 signal lines	

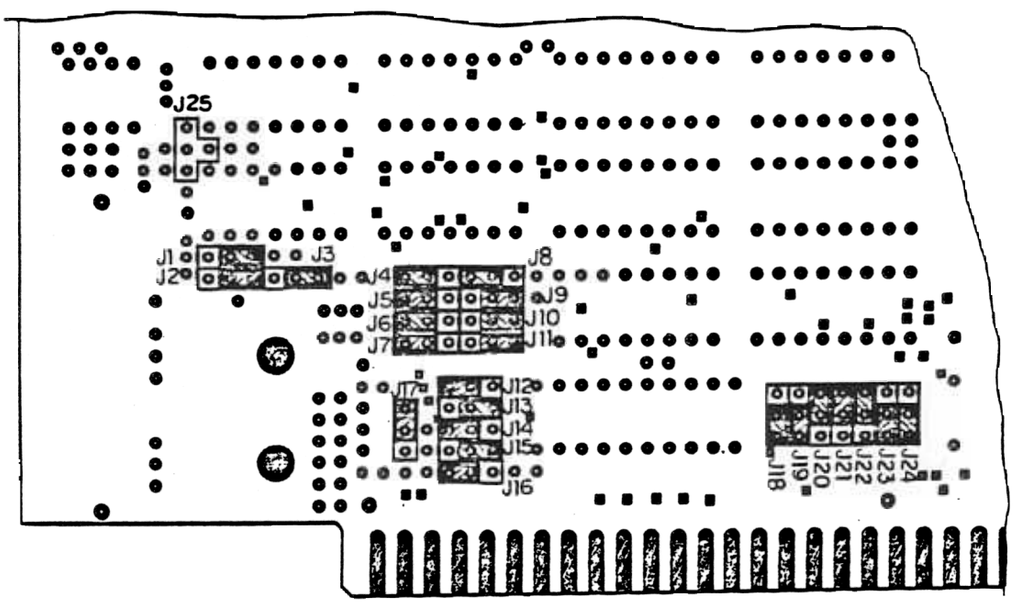

Figure A-1. Location of Jumpers Showing Factory Settings

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Appendix B - HINTS ON UTILITY SOFTWARE AND PARITY BYTE

(Not Released in Preliminary Manual)

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Appendix C - SAMPLE DRIVER SOFTWARE

(Not Released in Preliminary Manual)

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Appendix D - SYSTEM MEMORY BASE ADDRESS TABLES

BASE ADDRESS SETTING FOR V-RAM AS SYSTEM MEMORY

64K Boundary Base Address	J4	J5	J6	J7	J8	J9	J10	
000000H	Left	Left	Left	Left	Left	Left	Left	Left
010000H	Left	Left	Left	Left	Left	Left	Left	Right
020000H	Left	Left	Left	Left	Left	Left	Right	Left
030000H	Left	Left	Left	Left	Left	Left	Right	Right
040000H	Left	Left	Left	Left	Left	Right	Left	Left
050000H	Left	Left	Left	Left	Left	Right	Left	Right
060000H	Left	Left	Left	Left	Left	Right	Right	Left
070000H	Left	Left	Left	Left	Left	Right	Right	Right
080000H	Left	Left	Left	Left	Right	Left	Left	Left
090000H	Left	Left	Left	Left	Right	Left	Left	Right
0A0000H	Left	Left	Left	Left	Right	Left	Right	Left
0B0000H	Left	Left	Left	Left	Right	Left	Right	Right
0C0000H	Left	Left	Left	Left	Right	Right	Left	Left
0D0000H	Left	Left	Left	Left	Right	Right	Left	Right
0E0000H	Left	Left	Left	Left	Right	Right	Right	Left
0F0000H	Left	Left	Left	Left	Right	Right	Right	Right
100000H	Left	Left	Left	Right	Left	Left	Left	Left
110000H	Left	Left	Left	Right	Left	Left	Left	Right
120000H	Left	Left	Left	Right	Left	Left	Right	Left
130000H	Left	Left	Left	Right	Left	Left	Right	Right
140000H	Left	Left	Left	Right	Left	Right	Left	Left
150000H	Left	Left	Left	Right	Left	Right	Left	Right
160000H	Left	Left	Left	Right	Left	Right	Right	Left
170000H	Left	Left	Left	Right	Left	Right	Right	Right
180000H	Left	Left	Left	Right	Right	Left	Left	Left
190000H	Left	Left	Left	Right	Right	Left	Left	Right
1A0000H	Left	Left	Left	Right	Right	Left	Right	Left
1B0000H	Left	Left	Left	Right	Right	Left	Right	Right
1C0000H	Left	Left	Left	Right	Right	Right	Left	Left
1D0000H	Left	Left	Left	Right	Right	Right	Left	Right
1E0000H	Left	Left	Left	Right	Right	Right	Right	Left
1F0000H	Left	Left	Left	Right	Right	Right	Right	Right
200000H	Left	Left	Right	Left	Left	Left	Left	Left
210000H	Left	Left	Right	Left	Left	Left	Left	Right
220000H	Left	Left	Right	Left	Left	Left	Right	Left
230000H	Left	Left	Right	Left	Left	Left	Right	Right
240000H	Left	Left	Right	Left	Left	Right	Left	Left
250000H	Left	Left	Right	Left	Left	Right	Left	Right
260000H	Left	Left	Right	Left	Left	Right	Right	Left
270000H	Left	Left	Right	Left	Left	Right	Right	Right
280000H	Left	Left	Right	Left	Right	Left	Left	Left
290000H	Left	Left	Right	Left	Right	Left	Left	Right
2A0000H	Left	Left	Right	Left	Right	Left	Right	Left
2B0000H	Left	Left	Right	Left	Right	Left	Right	Right
2C0000H	Left	Left	Right	Left	Right	Right	Left	Left
2D0000H	Left	Left	Right	Left	Right	Right	Left	Right
2E0000H	Left	Left	Right	Left	Right	Right	Right	Left
2F0000H	Left	Left	Right	Left	Right	Right	Right	Right
300000H	Left	Left	Right	Right	Left	Left	Left	Left

Appendix D - SYSTEM MEMORY BASE ADDRESS TABLES

64K Boundary Base Address	J4	J5	J6	J7	J8	J9	J10	J11
310000H	Left	Left	Right	Right	Left	Left	Left	Right
320000H	Left	Left	Right	Right	Left	Left	Right	Left
330000H	Left	Left	Right	Right	Left	Left	Right	Right
340000H	Left	Left	Right	Right	Left	Right	Left	Left
350000H	Left	Left	Right	Right	Left	Right	Left	Right
360000H	Left	Left	Right	Right	Left	Right	Right	Left
370000H	Left	Left	Right	Right	Left	Right	Right	Right
380000H	Left	Left	Right	Right	Right	Left	Left	Left
390000H	Left	Left	Right	Right	Right	Left	Left	Right
3A0000H	Left	Left	Right	Right	Right	Left	Right	Left
3B0000H	Left	Left	Right	Right	Right	Left	Right	Right
3C0000H	Left	Left	Right	Right	Right	Right	Left	Left
3D0000H	Left	Left	Right	Right	Right	Right	Left	Right
3E0000H	Left	Left	Right	Right	Right	Right	Right	Left
3F0000H	Left	Left	Right	Right	Right	Right	Right	Right
400000H	Left	Right	Left	Left	Left	Left	Left	Left
410000H	Left	Right	Left	Left	Left	Left	Left	Right
420000H	Left	Right	Left	Left	Left	Left	Right	Left
430000H	Left	Right	Left	Left	Left	Left	Right	Right
440000H	Left	Right	Left	Left	Left	Right	Left	Left
450000H	Left	Right	Left	Left	Left	Right	Left	Right
460000H	Left	Right	Left	Left	Left	Right	Right	Left
470000H	Left	Right	Left	Left	Left	Right	Right	Right
480000H	Left	Right	Left	Left	Right	Left	Left	Left
490000H	Left	Right	Left	Left	Right	Left	Left	Right
4A0000H	Left	Right	Left	Left	Right	Left	Right	Left
4B0000H	Left	Right	Left	Left	Right	Left	Right	Right
4C0000H	Left	Right	Left	Left	Right	Right	Left	Left
4D0000H	Left	Right	Left	Left	Right	Right	Left	Right
4E0000H	Left	Right	Left	Left	Right	Right	Right	Left
4F0000H	Left	Right	Left	Left	Right	Right	Right	Right
500000H	Left	Right	Left	Right	Left	Left	Left	Left
510000H	Left	Right	Left	Right	Left	Left	Left	Right
520000H	Left	Right	Left	Right	Left	Left	Right	Left
530000H	Left	Right	Left	Right	Left	Left	Right	Right
540000H	Left	Right	Left	Right	Left	Right	Left	Left
550000H	Left	Right	Left	Right	Left	Right	Left	Right
560000H	Left	Right	Left	Right	Left	Right	Right	Left
570000H	Left	Right	Left	Right	Left	Right	Right	Right
580000H	Left	Right	Left	Right	Right	Left	Left	Left
590000H	Left	Right	Left	Right	Right	Left	Left	Right
5A0000H	Left	Right	Left	Right	Right	Left	Right	Left
5B0000H	Left	Right	Left	Right	Right	Left	Right	Right
5C0000H	Left	Right	Left	Right	Right	Right	Left	Left
5D0000H	Left	Right	Left	Right	Right	Right	Left	Right
5E0000H	Left	Right	Left	Right	Right	Right	Right	Left
5F0000H	Left	Right	Left	Right	Right	Right	Right	Right
600000H	Left	Right	Right	Left	Left	Left	Left	Left
610000H	Left	Right	Right	Left	Left	Left	Left	Right

Appendix D - SYSTEM MEMORY BASE ADDRESS TABLES

64K Boundary Base Address	J4	J5	J6	J7	J8	J9	J10	J11
620000H	Left	Right	Right	Left	Left	Left	Right	Left
630000H	Left	Right	Right	Left	Left	Left	Right	Right
640000H	Left	Right	Right	Left	Left	Right	Left	Left
650000H	Left	Right	Right	Left	Left	Right	Left	Right
660000H	Left	Right	Right	Left	Left	Right	Right	Left
670000H	Left	Right	Right	Left	Left	Right	Right	Right
680000H	Left	Right	Right	Left	Right	Left	Left	Left
690000H	Left	Right	Right	Left	Right	Left	Left	Right
6A0000H	Left	Right	Right	Left	Right	Left	Right	Left
6B0000H	Left	Right	Right	Left	Right	Left	Right	Right
6C0000H	Left	Right	Right	Left	Right	Right	Left	Left
6D0000H	Left	Right	Right	Left	Right	Right	Left	Right
6E0000H	Left	Right	Right	Left	Right	Right	Right	Left
6F0000H	Left	Right	Right	Left	Right	Right	Right	Right
700000H	Left	Right	Right	Right	Left	Left	Left	Left
710000H	Left	Right	Right	Right	Left	Left	Left	Right
720000H	Left	Right	Right	Right	Left	Left	Right	Left
730000H	Left	Right	Right	Right	Left	Left	Right	Right
740000H	Left	Right	Right	Right	Left	Right	Left	Left
750000H	Left	Right	Right	Right	Left	Right	Left	Right
760000H	Left	Right	Right	Right	Left	Right	Right	Left
770000H	Left	Right	Right	Right	Left	Right	Right	Right
780000H	Left	Right	Right	Right	Right	Left	Left	Left
790000H	Left	Right	Right	Right	Right	Left	Left	Right
7A0000H	Left	Right	Right	Right	Right	Left	Right	Left
7B0000H	Left	Right	Right	Right	Right	Left	Right	Right
7C0000H	Left	Right	Right	Right	Right	Right	Left	Left
7D0000H	Left	Right	Right	Right	Right	Right	Left	Right
7E0000H	Left	Right	Right	Right	Right	Right	Right	Left
7F0000H	Left	Right	Right	Right	Right	Right	Right	Right
800000H	Left	~~Right~~	Left	Left	Left	~~Left~~ Left	Left	Left
810000H	Right	Left	Left	Left	Left	Left	Left	Right
820000H	Right	Left	Left	Left	Left	Left	Right	Left
830000H	Right	Left	Left	Left	Left	Left	Right	Right
840000H	Right	Left	Left	Left	Left	Right	Left	Left
850000H	Right	Left	Left	Left	Left	Right	Left	Right
860000H	Right	Left	Left	Left	Left	Right	Right	Left
870000H	Right	Left	Left	Left	Left	Right	Right	Right
880000H	Right	Left	Left	Left	Right	Left	Left	Left
890000H	Right	Left	Left	Left	Right	Left	Left	Right
8A0000H	Right	Left	Left	Left	Right	Left	Right	Left
8B0000H	Right	Left	Left	Left	Right	Left	Right	Right
8C0000H	Right	Left	Left	Left	Right	Right	Left	Left
8D0000H	Right	Left	Left	Left	Right	Right	Left	Right
8E0000H	Right	Left	Left	Left	Right	Right	Right	Left
8F0000H	Right	Left	Left	Left	Right	Right	Right	Right
900000H	Right	Left	Left	Right	Left	Left	Left	Left
910000H	Right	Left	Left	Right	Left	Left	Left	Right
920000H	Right	Left	Left	Right	Left	Left	Right	Left

Appendix D - SYSTEM MEMORY BASE ADDRESS TABLES

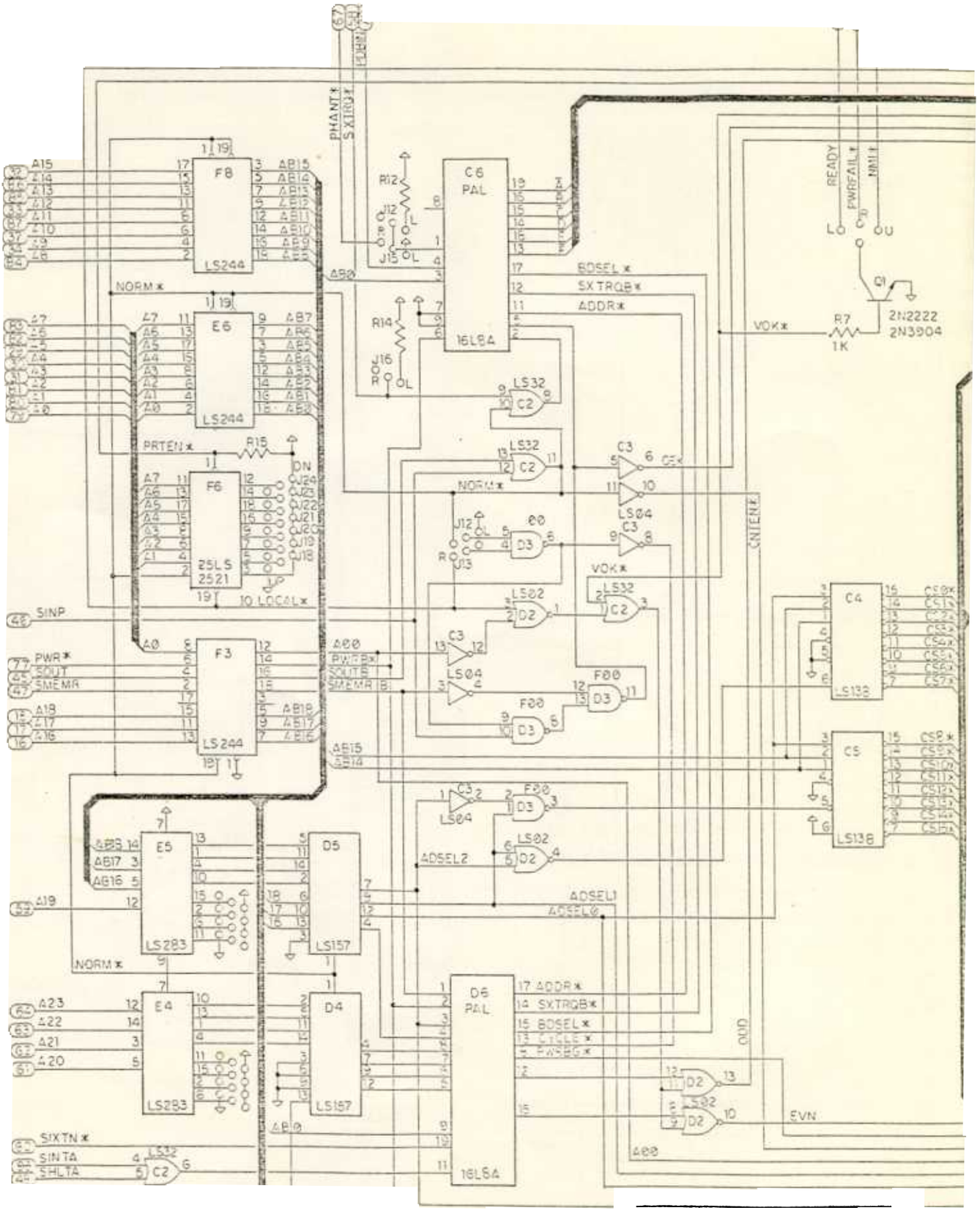
64K Boundary Base Address	J4	J5	J6	J7	J8	J9	J10	J11
930000H	Right	Left	Left	Right	Left	Left	Right	Right
940000H	Right	Left	Left	Right	Left	Right	Left	Left
950000H	Right	Left	Left	Right	Left	Right	Left	Right
960000H	Right	Left	Left	Right	Left	Right	Right	Left
970000H	Right	Left	Left	Right	Left	Right	Right	Right
980000H	Right	Left	Left	Right	Right	Left	Left	Left
990000H	Right	Left	Left	Right	Right	Left	Left	Right
9A0000H	Right	Left	Left	Right	Right	Left	Right	Left
9B0000H	Right	Left	Left	Right	Right	Left	Right	Right
9C0000H	Right	Left	Left	Right	Right	Right	Left	Left
9D0000H	Right	Left	Left	Right	Right	Right	Left	Right
9E0000H	Right	Left	Left	Right	Right	Right	Right	Left
9F0000H	Right	Left	Left	Right	Right	Right	Right	Right
A00000H	Right	Left	Right	Left	Left	Left	Left	Left
A10000H	Right	Left	Right	Left	Left	Left	Left	Right
A20000H	Right	Left	Right	Left	Left	Left	Right	Left
A30000H	Right	Left	Right	Left	Left	Left	Right	Right
A40000H	Right	Left	Right	Left	Left	Right	Left	Left
A50000H	Right	Left	Right	Left	Left	Right	Left	Right
A60000H	Right	Left	Right	Left	Left	Right	Right	Left
A70000H	Right	Left	Right	Left	Left	Right	Right	Right
A80000H	Right	Left	Right	Left	Right	Left	Left	Left
A90000H	Right	Left	Right	Left	Right	Left	Left	Right
AA0000H	Right	Left	Right	Left	Right	Left	Right	Left
AB0000H	Right	Left	Right	Left	Right	Left	Right	Right
AC0000H	Right	Left	Right	Left	Right	Right	Left	Left
AD0000H	Right	Left	Right	Left	Right	Right	Left	Right
AE0000H	Right	Left	Right	Left	Right	Right	Right	Left
AF0000H	Right	Left	Right	Left	Right	Right	Right	Right
B00000H	Right	Left	Right	Right	Left	Left	Left	Left
B10000H	Right	Left	Right	Right	Left	Left	Left	Right
B20000H	Right	Left	Right	Right	Left	Left	Right	Left
B30000H	Right	Left	Right	Right	Left	Left	Right	Right
B40000H	Right	Left	Right	Right	Left	Right	Left	Left
B50000H	Right	Left	Right	Right	Left	Right	Left	Right
B60000H	Right	Left	Right	Right	Left	Right	Right	Left
B70000H	Right	Left	Right	Right	Left	Right	Right	Right
B80000H	Right	Left	Right	Right	Right	Left	Left	Left
B90000H	Right	Left	Right	Right	Right	Left	Left	Right
BA0000H	Right	Left	Right	Right	Right	Left	Right	Left
BB0000H	Right	Left	Right	Right	Right	Left	Right	Right
BC0000H	Right	Left	Right	Right	Right	Right	Left	Left
BD0000H	Right	Left	Right	Right	Right	Right	Left	Right
BE0000H	Right	Left	Right	Right	Right	Right	Right	Left
BF0000H	Right	Left	Right	Right	Right	Right	Right	Right
C00000H	Right	Right	Left	Left	Left	Left	Left	Left
C10000H	Right	Right	Left	Left	Left	Left	Left	Right
C20000H	Right	Right	Left	Left	Left	Left	Right	Left
C30000H	Right	Right	Left	Left	Left	Left	Right	Right

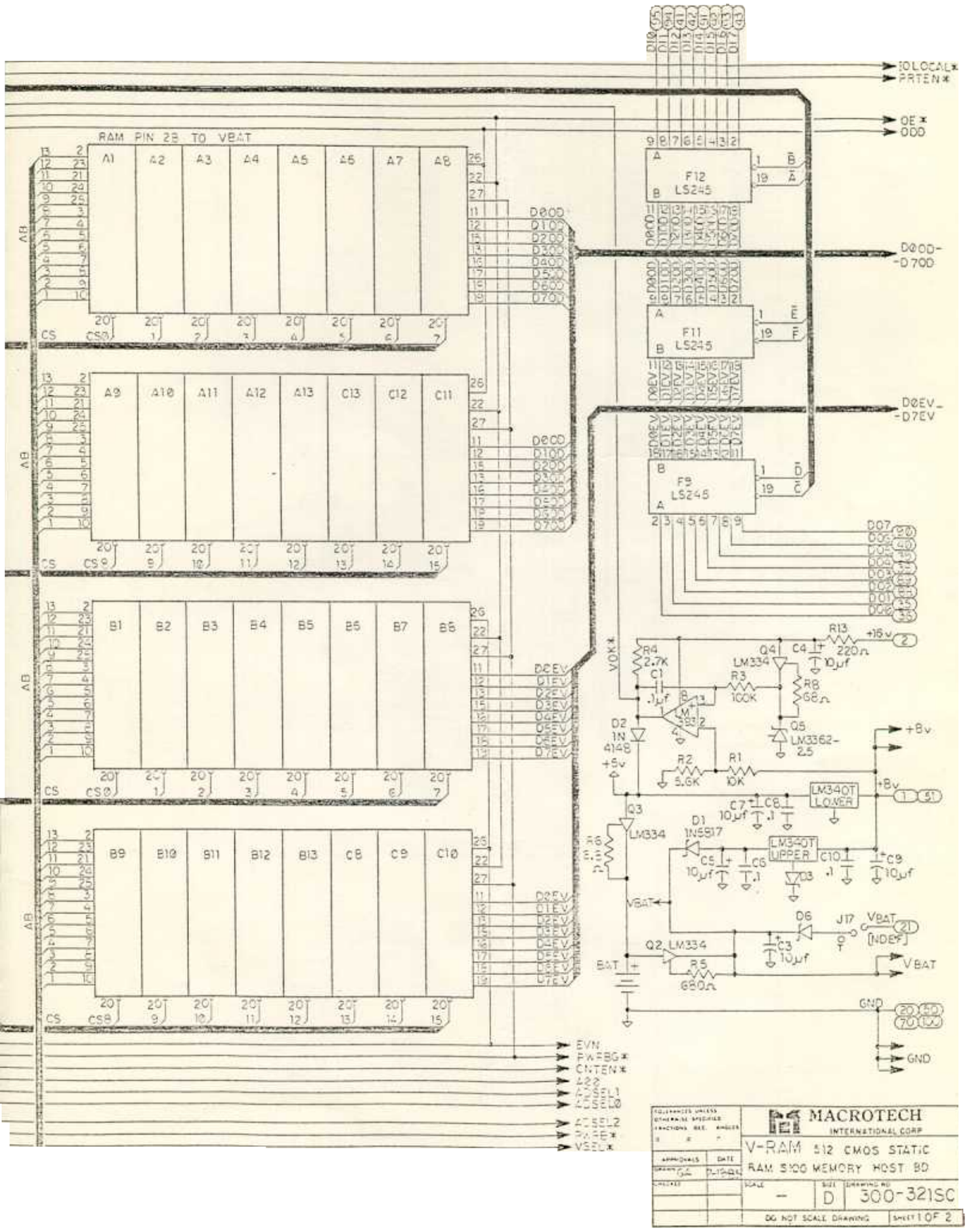
Appendix D - SYSTEM MEMORY BASE ADDRESS TABLES

64K Boundary Base Address	J4	J5	J6	J7	J8	J9	J10	
C40000H	Right	Right	Left	Left	Left	Right	Left	Left
C50000H	Right	Right	Left	Left	Left	Right	Left	Right
C60000H	Right	Right	Left	Left	Left	Right	Right	Left
C70000H	Right	Right	Left	Left	Left	Right	Right	Right
C80000H	Right	Right	Left	Left	Right	Left	Left	Left
C90000H	Right	Right	Left	Left	Right	Left	Left	Right
CA0000H	Right	Right	Left	Left	Right	Left	Right	Left
CB0000H	Right	Right	Left	Left	Right	Left	Right	Right
CC0000H	Right	Right	Left	Left	Right	Right	Left	Left
CD0000H	Right	Right	Left	Left	Right	Right	Left	Right
CE0000H	Right	Right	Left	Left	Right	Right	Right	Left
CF0000H	Right	Right	Left	Left	Right	Right	Right	Right
D00000H	Right	Right	Left	Right	Left	Left	Left	Left
D10000H	Right	Right	Left	Right	Left	Left	Left	Right
D20000H	Right	Right	Left	Right	Left	Left	Right	Left
D30000H	Right	Right	Left	Right	Left	Left	Right	Right
D40000H	Right	Right	Left	Right	Left	Right	Left	Left
D50000H	Right	Right	Left	Right	Left	Right	Left	Right
D60000H	Right	Right	Left	Right	Left	Right	Right	Left
D70000H	Right	Right	Left	Right	Left	Right	Right	Right
D80000H	Right	Right	Left	Right	Right	Left	Left	Left
D90000H	Right	Right	Left	Right	Right	Left	Left	Right
DA0000H	Right	Right	Left	Right	Right	Left	Right	Left
DB0000H	Right	Right	Left	Right	Right	Left	Right	Right
DC0000H	Right	Right	Left	Right	Right	Right	Left	Left
DD0000H	Right	Right	Left	Right	Right	Right	Left	Right
DE0000H	Right	Right	Left	Right	Right	Right	Right	Left
DF0000H	Right	Right	Left	Right	Right	Right	Right	Right
E00000H	Right	Right	Right	Left	Left	Left	Left	Left
E10000H	Right	Right	Right	Left	Left	Left	Left	Right
E20000H	Right	Right	Right	Left	Left	Left	Right	Left
E30000H	Right	Right	Right	Left	Left	Left	Right	Right
E40000H	Right	Right	Right	Left	Left	Right	Left	Left
E50000H	Right	Right	Right	Left	Left	Right	Left	Right
E60000H	Right	Right	Right	Left	Left	Right	Right	Left
E70000H	Right	Right	Right	Left	Left	Right	Right	Right
E80000H	Right	Right	Right	Left	Right	Left	Left	Left
E90000H	Right	Right	Right	Left	Right	Left	Left	Right
EA0000H	Right	Right	Right	Left	Right	Left	Right	Left
EB0000H	Right	Right	Right	Left	Right	Left	Right	Right
EC0000H	Right	Right	Right	Left	Right	Right	Left	Left
ED0000H	Right	Right	Right	Left	Right	Right	Left	Right
EE0000H	Right	Right	Right	Left	Right	Right	Right	Left
EF0000H	Right	Right	Right	Left	Right	Right	Right	Right
F00000H	Right	Right	Right	Right	Left	Left	Left	Left
F10000H	Right	Right	Right	Right	Left	Left	Left	Right
F20000H	Right	Right	Right	Right	Left	Left	Right	Left
F30000H	Right	Right	Right	Right	Left	Left	Right	Right
F40000H	Right	Right	Right	Right	Left	Right	Left	Left

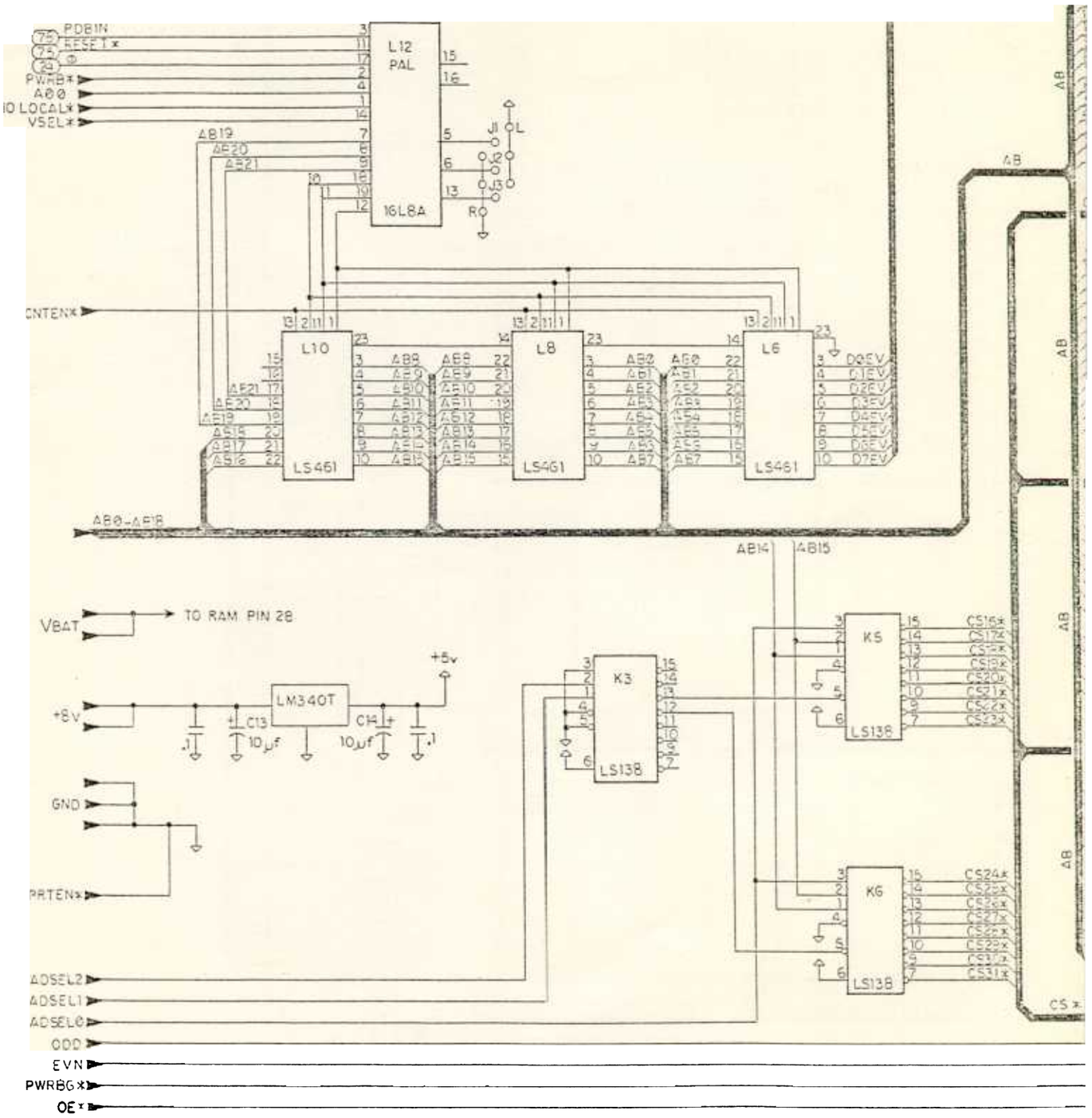
Appendix D - SYSTEM MEMORY BASE ADDRESS TABLES

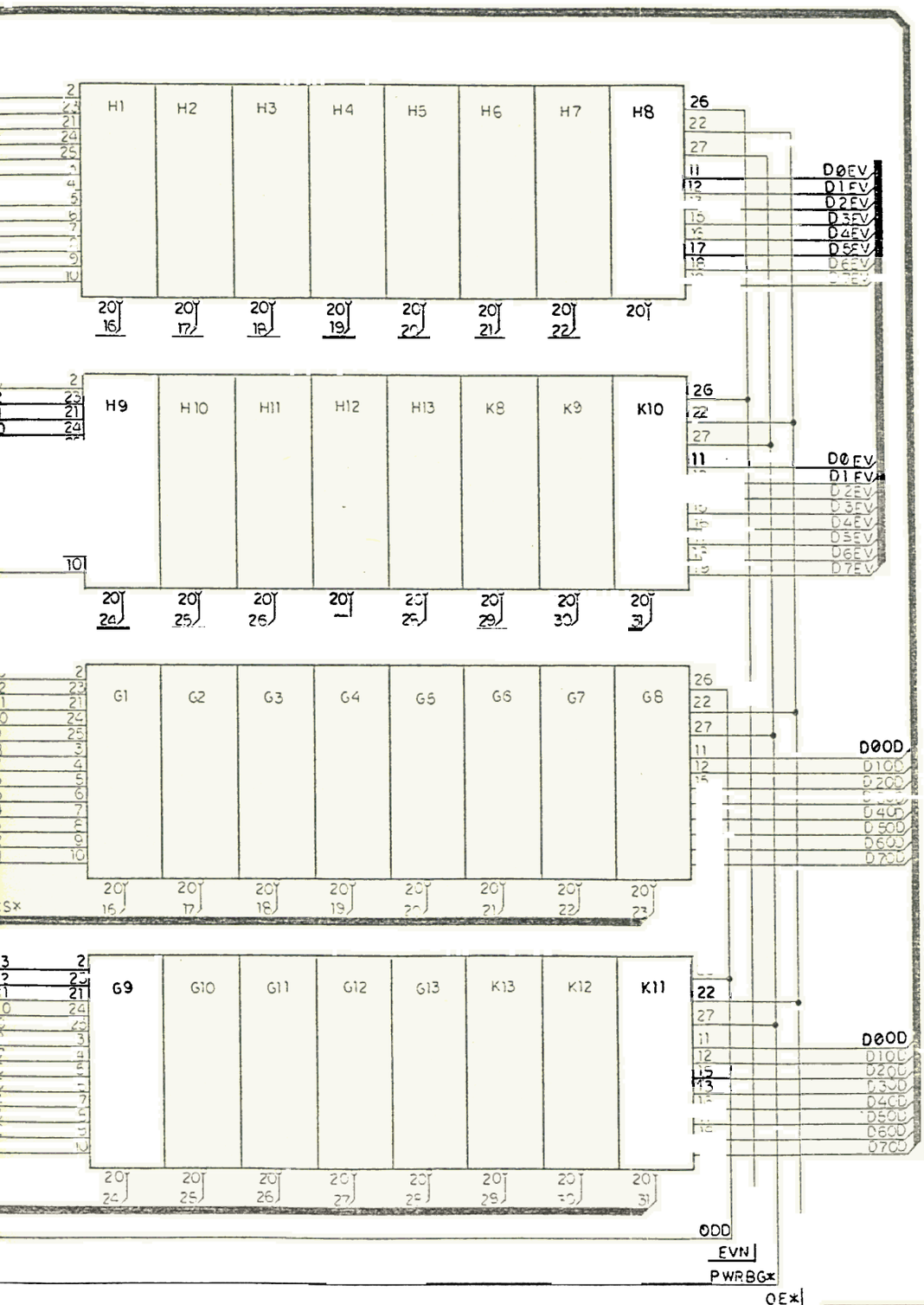
64K Boundary Base Address	J4	J5	J6	J7	J8	J9	J10	J11
F50000H	Right	Right	Right	Right	Left	Right	Left	Right
F60000H	Right	Right	Right	Right	Left	Right	Right	Left
F70000H	Right	Right	Right	Right	Left	Right	Right	Right
F80000H	Right	Right	Right	Right	Right	Left	Left	Left
F90000H	Right	Right	Right	Right	Right	Left	Left	Right
FA0000H	Right	Right	Right	Right	Right	Left	Right	Left
FB0000H	Right	Right	Right	Right	Right	Left	Right	Right
FC0000H	Right	Right	Right	Right	Right	Right	Left	Left
FD0000H	Right	Right	Right	Right	Right	Right	Left	Right
FE0000H	Right	Right	Right	Right	Right	Right	Right	Left
FF0000H	Right	Right	Right	Right	Right	Right	Right	Right


PHANT*
SXTRQB*
F8
LS244
E6
LS244
F6
25LS
2521
F3
LS244
E5
LS283
E4
LS283
D5
LS157
D4
LS157
C6
PAL
16L8A
D6
PAL
16L8A
R12
R14
R15
R16
R7
1K
J12
J15
J16
J13
LS32
LS04
LS02
F00
C3
D2
D3
C2
C4
C5
LS138
Q1
2N2222
2N3904
READY
PWRFAIL*
VOK*
NORM*
PRTEN*
SINP
PWR*
SOUT
SMEMR
SIXTN*
SINTA
SHLTA
ADSEL2
ADSEL1
ADSEL0
BDSEL*
ADDR*
CNTENE*
EVN
ODD
LOCAL*



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES	MACROTECH INTERNATIONAL CORP	
APPROVALS / DATE	V-RAM 512 CMOS STATIC RAM S100 MEMORY HOST BD	
DRAWN GA 11-19-81	SCALE –	SIZE D / DRAWING NO 300-321SC
	DO NOT SCALE DRAWING	SHEET 1 OF 2


D00D - D70D
PDBIN
RESET*
Φ
PWRB*
A00
IO LOCAL*
VSEL*
L12
PAL
16L8A
J1
J2
J3
L
R0
AB19
AB20
AB21
CNTEN*
L10
L8
L6
LS461
D0EV
D1EV
D2EV
D3EV
D4EV
D5EV
D6EV
D7EV
AB0-AB19
AB14
AB15
VBAT
TO RAM PIN 28
+8V
LM340T
C13
10µf
C14
10µf
+5v
GND
PRTEN*
K3
K5
K6
LS138
CS16*
CS17*
CS18*
CS19*
CS20*
CS21*
CS22*
CS23*
CS24*
CS25*
CS26*
CS27*
CS28*
CS29*
CS30*
CS31*
CS*
AB
ADSEL2
ADSEL1
ADSEL0
ODD
EVN
PWRBG*
OE*



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES	MACROTECH INTERNATIONAL CORP	
APPROVALS / DATE	V-RAM 512K CMOS STATIC RAM S-100 MEMORY ADAPTER BD	
DRAWN GA	SCALE —	SIZE D
CHECKED	DRAWING NO 300-324SC	
DO NOT SCALE DRAWING	SHEET 2 OF 2	