MANUAL FOR Boards with
BD- 1598

The Ithaca InterSystems ADDA-8

Edition 1.0

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1.0 INTRODUCTION

This manual describes the Ithaca InterSystems ADDA-8 circuit board. The board is shipped from the company in a standard configuration. The board can be reconfigured by the user to provide the features required for specific applications.

Like all InterSystems products, the ADDA-8 is completely tested prior to shipment, and should provide years of trouble-free service. It is important, however, that the board be inspected upon receiving, and in any event service may some day be required. The InterSystems Policies manual contains information about these subjects.

The manual includes an introduction to the board's features, a functional description of the board, and instructions for preparing the board for operation in a system. The manual also contains detailed circuit descriptions, alignment procedures, and the parts list.

1.1 PHYSICAL DESCRIPTION

The ADDA-8 is a standard 5 by 10 inch (12.7 by 25.4 cm), S-100 bus, plug-in circuit board. The board has a 50-pin top edge connector for interfacing with eight input and eight output analog signal lines. Test points are provided for each analog input and output line. Ground planes have been used in all available space and analog lines have been isolated from digital lines in an effort to eliminate problems caused by noise. Trim pots are provided for all critical board alignment adjustments.

1.2 STANDARD FEATURES

The ADDA-8 features include:

* Eight multiplexed analog to eight-bit digital (A/D) channels and eight independent eight-bit digital to analog (D/A) channels are provided.

* A/D input range is +5 to -5 Volts.

* D/A output range is +5 to -5 Volts.

* A/D sampling in excess of 20 kHz is possible based

on a 25 microsecond typical (30 microsecond maximum) conversion time for the A/D converter, 5 microsecond typical sample/hold acquisition time, plus 2 microsecond MUX switching time.

* D/A converters have a typical settling time of 2.5 microseconds.

* The real time clock (RTC) is derived from CLOCK* on the S-100 bus. The RTC has a 32-bit time constant.

* The board can be either I/O or memory mapped, with selectable 8- or 16-bit address decoding.

* Interrupt driven operation is possible in two modes (software programmable):

    * The interrupt is requested when the A/D circuit finishes a conversion.
    * The interrupt is requested when the RTC times out.

* The interrupt flip flop may be cleared whenever the board is addressed to assist in interrupt driven operation.

* A/D may be started when the RTC times out, or under program control.

* One or two wait states may be added at RTC accesses.

* A status port allows the interrupt request, RTC output, or A/D conversion status to be polled.

* A control port allows the user to configure the board under software control.

* Phantom output allows the board to occupy the same address space as memory boards equipped with Phantom inputs.
* Boards are completely aligned prior to shipment.

2.0 FUNCTIONAL DESCRIPTION

This section of the ADDA-8 manual describes the basic functions of the circuit card. Actual preparation of the board for operation is described in section 3.0. Detailed circuit descriptions are provided in section 4.0 of the manual. The following functional areas are described in this section:

* Bus interface and board addressing
* Control port
* Real time clock
* Analog to digital conversion
* Digital to analog conversion
* Interrupt driven operation
* Polled operation

2.1 BUS INTERFACE AND BOARD ADDRESSING

The ADDA-8 can be configured for either I/O mapped addressing or for memory mapped addressing. Also, the board can be configured for either 8-bit or 16-bit addressing. This allows the board to function in either an 8-bit or 16-bit I/O mapped mode or in the 16-bit memory mapped mode. The board uses the S-100 PHANTOM* line, enabling the board to be memory mapped in the same address space as any system memory board that can decode the Phantom line.

The board address map is defined as follows:

Output		Input	
Port	Function	Port	Function
0	Digital/Analog 0	8	Read Status
1	Digital/Analog 1	C	Read A/D
2	Digital/Analog 2		
3	Digital/Analog 3		
4	Digital/Analog 4		
5	Digital/Analog 5		
6	Digital/Analog 6		
7	Digital/Analog 7		
8	8253 Data Port, Counter 0		
9	8253 Data Port, Counter 1		
A	8253 Data Port, Counter 2		
B	8253 Control Port		
C	ADDA-8 Control Port		

2.2 ADDA-8 CONTROL PORT

A control port (at location C in the board address space) allows several board functions to be under software control. The control port is defined as follows:

Bit	Function
0	MUX address 0
1	MUX address 1
2	MUX address 2
3	MUX address change strobe
4	Start A/D conversion strobe
5	Enable RTC to generate interrupt
6	Enable RTC to start A/D, and A/D to initiate interrupt
7	Interrupt reset

The control port contains the A/D multiplex address on its lower three bits (0-2). Bit 3 acts as the address change strobe. The MUX address is changed when the address change strobe is high. Bit 4, if high, starts the A/D converter whenever the control port is updated. Bit 5 set high enables the RTC time out to initiate the interrupt request. Bit 6 set high enables the RTC time out to initiate A/D conversion. A/D then initiates an interrupt request. Bit 7 resets the interrupt request flip-flop. Bits 4 through 7 in the control port may be changed without affecting the MUX address because the MUX address is only changed when the MUX address strobe (bit 3) is high.

2.3 REAL TIME CLOCK

The real time clock uses two of the three 16-bit timers available in the 8253 programmable interval timer. The two counters are cascaded to form a 32-bit time constant generator. See Figure 2. Both counters are programmed as rate generators, and control words and time constants are loaded to each. A 2 MHz clock is input to the counter. The 2 MHz input clock is derived from the S-100 bus CLOCK*. The RTC count is automatically decremented once each clock period. When the counter reaches zero, the output goes low for one clock period. At the end of that period the RTC is automatically reloaded with the original count. The output of the RTC either sets the interrupt request flip-flop or starts the A/D conversion, depending on how the control port is set.

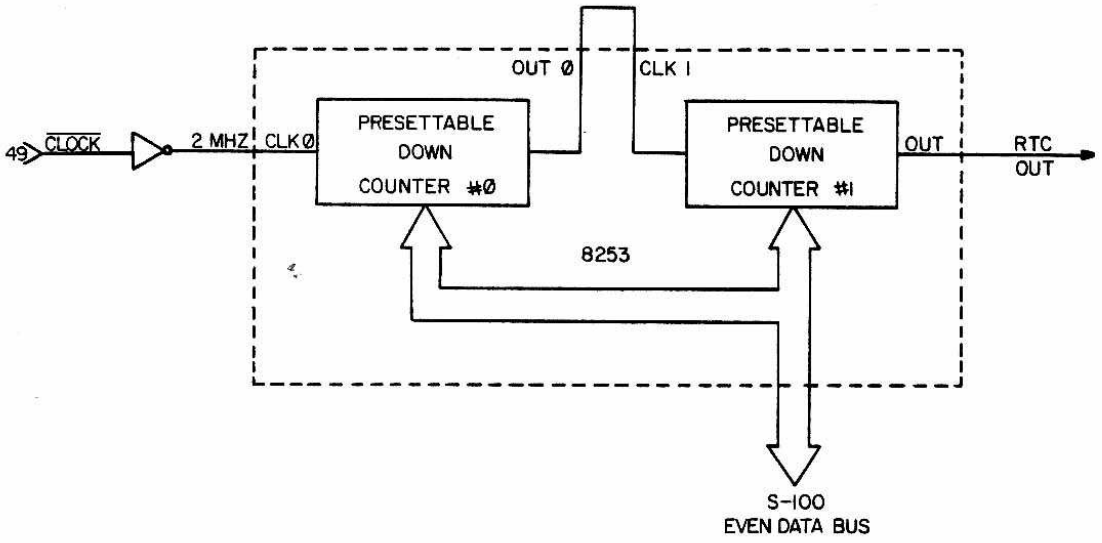


Figure 2 RTC

2.4 ANALOG TO DIGITAL CONVERSION

For the purpose of explanation, the process of A/D conversion is broken down into two steps: analog input, and A/D conversion and output. Refer to Figure 3.

Analog Input

The inputs to the eight channel single-ended multiplexer enter the board through the 50-pin top connector. The input signal range is -5 Volts to +5 Volts. No anti-aliasing filters are provided on the input lines. Signals input to the board must

be bandlimited and conditioned.

The desired input is selected by writing to the control port with bit 3 (MUX address strobe) high, and the three-bit MUX address on bits 0-2. The selected analog signal is output to the sample/hold amplifier (S/H). The S/H is normally in the sample mode, except during a conversion, when control logic puts it in the hold mode.

The S/H requires up to 5 microseconds to acquire the input signal after being switched from the hold mode back to the sample mode. It is up to the programmer to guarantee that enough time is allowed between the end of one conversion and the start of another. If the MUX address is changed an additional 2 microseconds must be provided to allow the address to settle. MUX switching time is saved by changing the MUX address during a conversion. The selected analog signal is output to the A/D converter.

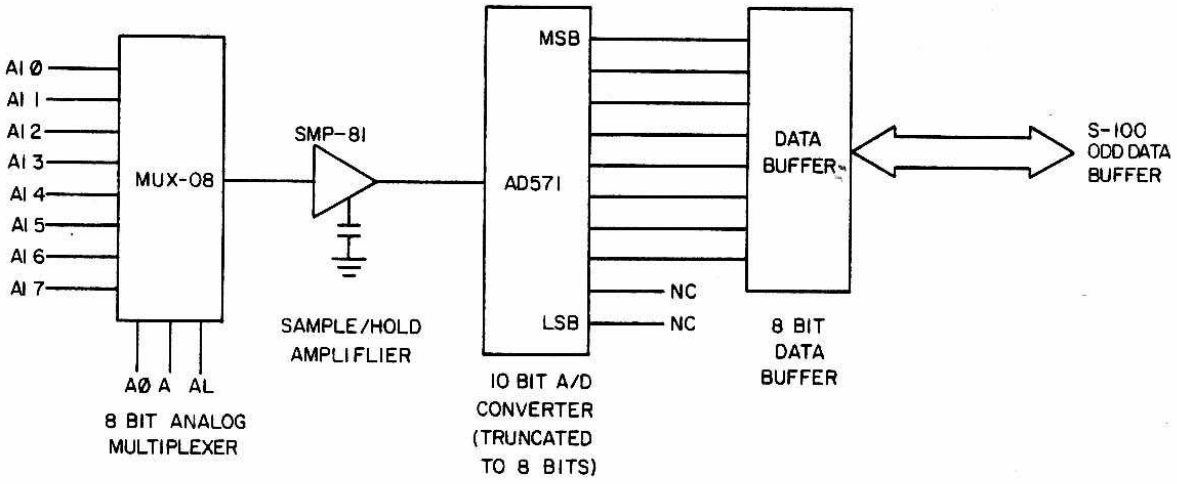


Figure 3 A/D conversion

Conversion

Input sampling may be controlled by software or by the RTC. RTC control ensures precise spacing of samples. If the control port is written to with bit 4 high, an A/D conversion is initiated. If bit 6 of the control port is high, the RTC output starts the A/D conversion.

The A/D has a maximum conversion time of 30 microseconds. The sample/hold amplifier requires 5 microseconds to settle after being placed in the sample mode. Sampling on a single channel may be done at sample rates greater than 29 kHz. If the MUX address is changed while a conversion is in progress, there is

no degradation in speed for multi-channel sampling. If the MUX address is changed before a conversion is initiated, an additional 2 microseconds is required.

The status port can be polled to determine when conversion is completed. The control port can be set so that the Conversion Complete signal sets the interrupt request flip-flop.

The digital output of the A/D converter is output on the S-100 Odd Data bus when the processor reads from port C of the board address space.

2.5 DIGITAL TO ANALOG CONVERSION

This section of the manual describes the D/A function. See Figure 4. Eight separate D/A converters are used on the ADDA-8. The use of individual converters allows high speed operation and avoids the problems inherent in multiplexed analog output schemes, such as the need for providing refresh for each channel and limiting the bandwidth of channels. Settling time of each D/A converter is approximately 2.5 microseconds. The D/A converters are self-contained. Each converter has a data latch, a voltage regulator and an output voltage amplifier. Each D/A channel is accessed at a different address with the board address space (locations 0 through 7). An individual channel is updated by writing to the proper address.

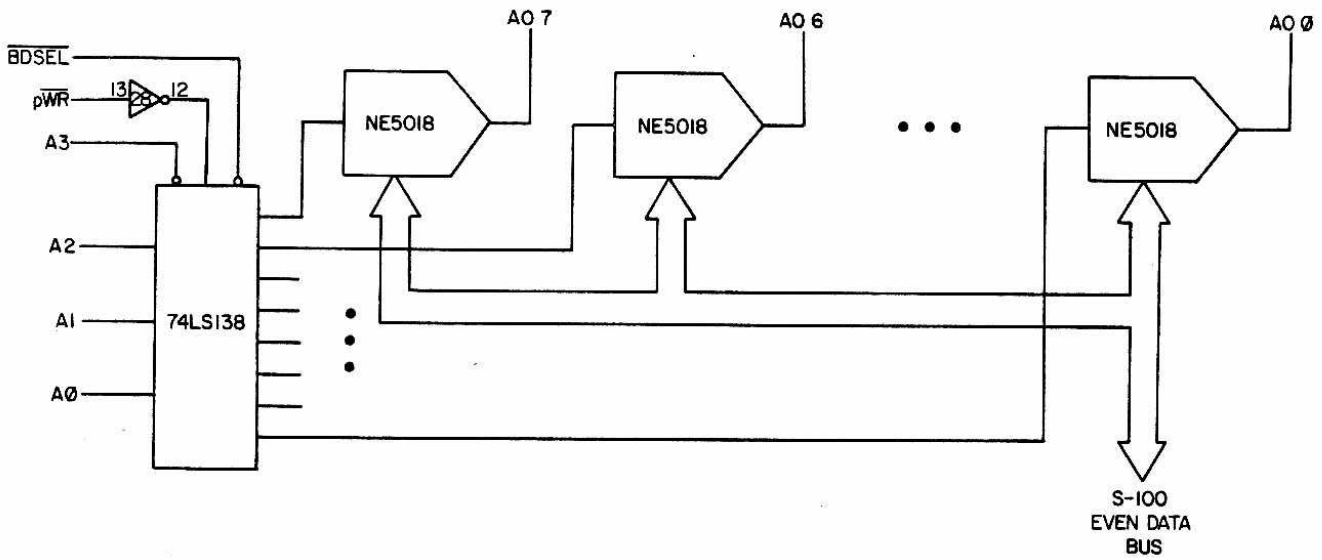


Figure 4 D/A conversion

2.6 INTERRUPT OPERATION

The ADDA-8 board is shipped with interrupts disabled. However, interrupt driven operation may be desirable when the time between samples is large; the system processor is not required to regularly poll the board to monitor infrequent events. The interrupt request flip-flop is clocked either by the A/D or by the RTC. Selection of the interrupt source is software controlled to allow dynamic reconfiguration of the board. The interrupt request output may be directed to any of the eight vectored interrupt lines on the S-100 bus. The interrupt request flip-flop is reset by writing to the control port with bit 7 high. Alternatively, with jumper J4 set to position A-B, reading or writing to any board address resets the flip-flop. The S-100 RESET* line also resets the flip-flop. Figure 5 is a block diagram of the reset control logic and interrupt control logic circuits.

A/D Initiates Interrupt Request

The A/D is selected to initiate the interrupt request by writing to the control port with bit 5 low and bit 6 high. In this mode, the RTC automatically starts the A/D conversion each time it times out. At the completion of the A/D conversion, the interrupt request flip-flop is set by the Conversion Complete signal. The processor reads the A/D at the interrupt. Samples occur at known intervals. Note that if the processor does not read the A/D before the next sample occurs, subsequent conversions are inhibited, and data is lost.

RTC Initiates Interrupt Request

The RTC is selected to initiate the interrupt request by writing to the control port with bit 5 high and bit 6 low. In this mode, the RTC time out signal sets the interrupt request flip-flop.

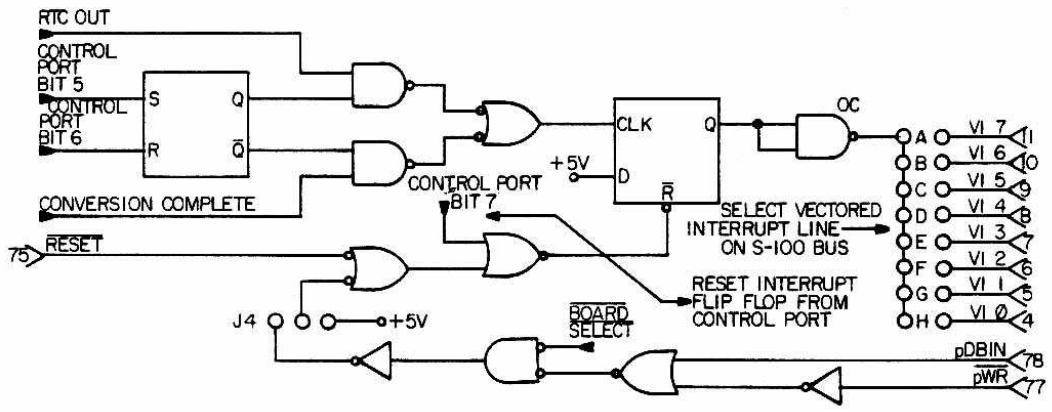


Figure 5 Interrupt control logic

2.7 POLLED OPERATION

Polled operation of the board may be advantageous in many situations. If an application requires short sampling intervals, polled operation may be faster than interrupt driven operations. An interrupt service routine that saves all registers takes approximately 100 microseconds to start servicing an interrupt. In polled operation the system processor polls the board's status port to determine when to read the A/D or start a conversion. The four lines of the status port are:

Bit	Signal
0	A/D Conversion Complete
1	RTC output
2	8253 OUT 2 output
7	Interrupt Request

3.0 BOARD SETUP

This section of the manual provides the information required to configure the ADDA-8 for use in a system. Instructions for board configuration are organized in functional groups. Specific instructions may refer to one or more jumper modifications, or to switch settings. A jumper summary and jumper definitions are provided to familiarize the user with jumper modification. Figure 6 shows the location of switches and jumpers on the board.

3.1 JUMPER SUMMARY AND DEFINITIONS

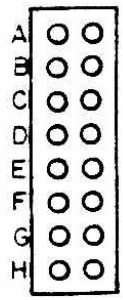
Jumper Summary

There are six jumper areas on the ADDA-8. Jumpers are used to prepare the board for use with different processors and processor speeds, and to select the method of board addressing. Each jumper area consists of one or more boxes containing a group of plated-through holes spaced 0.1 inches apart. To configure a jumper area one connection per box is made between adjacent holes. The connection is made by a shunt that slides onto 0.040 inch square posts that are soldered into the plated-through holes. The possible connections within a box are given letter names and are called "jumper positions". The letter names run A B C... from left to right or top to bottom, depending on the orientation of the jumper position.

Jumper Definitions

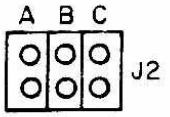
This section defines the function of each jumper.

J1 Selects the vectored interrupt line on which interrupt request is output. If interrupt-driven operation is not desired, remove the shunt at J1.



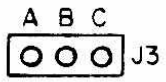
J1 A - VI7
J1 B - VI6
J1 C - VI5
J1 D - VI4
J1 E - VI3
J1 F - VI2
J1 G - VI1
J1 H - VI0

J2 J2 is set to determine how many wait states are generated when the RTC is addressed.

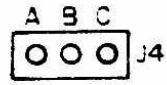


J2 A	Two wait states (6 MHz systems)
J2 B	One wait state (4 MHz systems)
J2 C	Zero wait states (2 MHz systems)

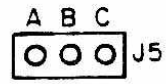
J3 Jumper J3 is set to determine whether the Phantom feature is enabled or disabled (in a memory mapped board - see J6 below). Jumper position A-B causes the Phantom line to be asserted when the board is selected. Jumper position B-C disables Phantom.



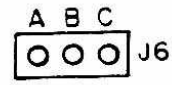
J4 Jumper position A-B causes the interrupt request flip-flop to be reset whenever the board is written to or read from. Jumper position B-C disables this option.



J5 Jumper position A-B enables the board to decode 8-bit addresses. Jumper position B-C enables the board to decode 16-bit addresses



J6 Jumper position A-B causes the board to be I/O mapped. Jumper position B-C causes the board to be memory mapped.



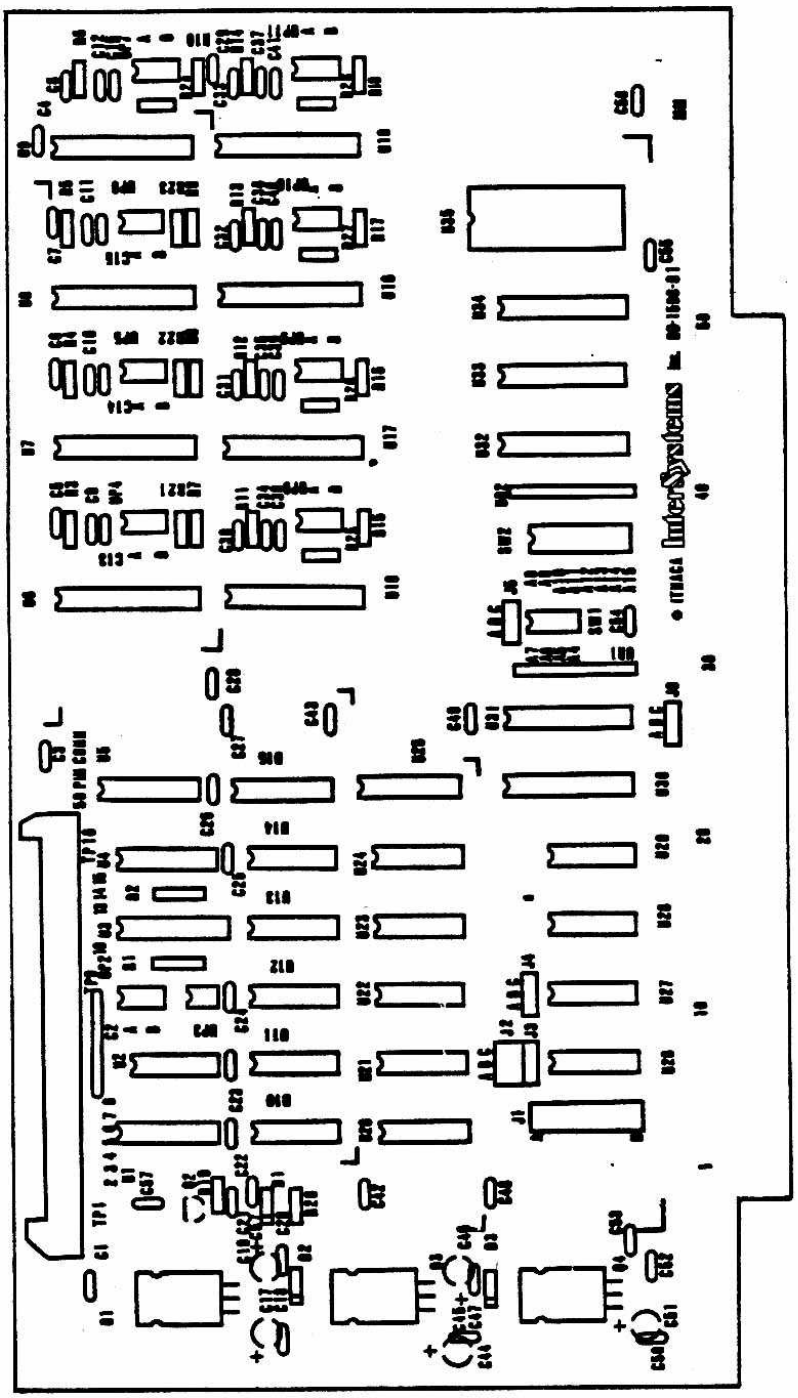


Figure 6 ADDA-8 board

3.2 ADDRESS SELECTION

The ADDA-8 can be configured for I/O or memory mapped operation, 8-bit or 16-bit addressing. J6 A-B selects I/O mapping. J6 B-C selects memory mapping.

J5 determines whether 8-bit or 16-bit addressing is decoded. J5 A-B selects 8-bit decoding for I/O mapped operation. J5 B-C selects 16-bit I/O or memory mapped address decoding.

DIP switches SW1 and SW2 are set to select the board's I/O or memory port address space. The ADDA-8 is set to occupy any 16 port space with an 0FH boundary base address; i.e., 00H, 0FH, 1FH, to FFH for eight bit I/O addressing, or 0000H, 000FH, 001FH, etc. for 16-bit I/O or memory addressing. Switches ~~SW1-4~~ through SW1-1 select address lines A4 through A7 respectively for both 8-bit and 16-bit addressing. Switches SW2-1 through SW2-8 select address lines A8 through A15 respectively for 16-bit addressing. An open switch corresponds to an address bit = 1. See Figure 7.

The Phantom signal allows an ADDA-8 configured for memory mapping to occupy the same memory space as a memory board that can decode the Phantom line. Jumper J3 A-B enables the Phantom line. J3 B-C disables the feature.

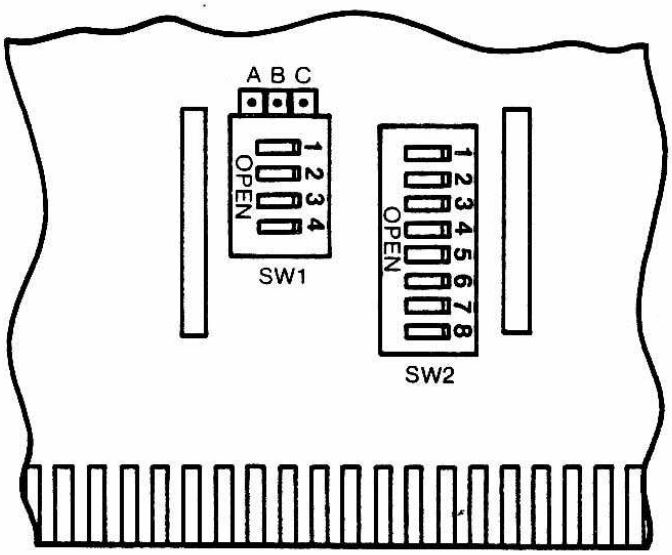


Figure 7 SW1 and SW2

3.3 WAIT STATES

Operation of the ADDA-8 in a system with a 2 MHz processor does not require a wait state. In a 4 MHz processor system, the board RTC requires the insertion of one wait state during RTC data transfers. Two wait states are required for operation in a 6 MHz system. J2 A requests two wait states. J2 B requests one wait state. J2 C requests zero wait states.

3.4 INTERRUPT DRIVEN OPERATION

Interrupt requests are initiated either at the RTC time out, or when an A/D conversion is completed. The selection of the interrupt request source is under software control, allowing dynamic reconfiguration of the board. When the A/D is selected to interrupt, the RTC automatically starts the A/D at RTC time out. In this mode, the processor only reads the A/D at an interrupt. Samples occur at known intervals because there is no variable delay between RTC time out and conversion initiation.

To enable the RTC to initiate interrupt, write to the control port with bit 5 high and bit 6 low. To allow the A/D to initiate the interrupt, write to the control port with bit 5 low and bit 6 high.

The interrupt flip-flop can be reset in one of three ways. The interrupt flip-flop is reset by a write to the control port with bit 7 high. Alternatively, J4 configured with jumper position A-B allows the flip-flop to be reset whenever the board is addressed, freeing the program of the responsibility. Whenever the S-100 reset line is active the interrupt flip-flop is reset.

Jumper J1 is configured to determine which vectored interrupt line is used to output the interrupt request. To disable interrupt controlled operation of the board remove the shunt from J1. See Figure 5.

3.5 POLLED OPERATION

Polled operation of the board may be desired. This section reviews the status port and suggests possible board setups for three modes of polled operation.

The board status port may be addressed at board addresses 8 through B. Bit 0 contains the Conversion Complete line of the A/D converter. The Conversion Complete is a latched output. It is reset when the A/D data is read.

Bit 1 contains the output of the RTC. Bit 2 contains the output of the third counter on the 8253 programmable interval timer. The RTC outputs are non-latched. After the processor detects that one of the status bits is true, it must wait for the flag to become false before testing to see if it is true again. Otherwise, the processor may take two samples when it should only take one.

Bit 7 of the status port contains the interrupt flip-flop output. The interrupt flip-flop is a latched output. It must be reset after a valid test before being tested again. Because it is latched, the processor need not sample the register repeatedly.

Conversion Complete Polled

In the first mode, the RTC is set up to start the A/D converter (write to control port with bit 6 high). The processor tests the Conversion Complete line until it is true. It then reads the A/D and acquires the sample. The processor may then start testing the Conversion Complete line again.

```
SETUP:  MVI A,40H
        OUT CNTRL          ;SET UP CONTROL PORT SO THAT
                           ;RTC STARTS A/D
        MVI C,ADDATA       ;PUT ADDRESS OF A/D INTO REG C
        LXI H,BUFFER       ;PUT STARTING ADDRESS OF DATA
                           ;BUFFER IN HL
        MVI B,NSAMPLES     ;PUT NUMBER OF SAMPLES INTO B
        CALL SETRTC        ;SET UP REAL TIME CLOCK
        CALL LOADRTC       ;LOAD TIME CONSTANTS INTO RTC
LOOP    IN STATUS          ;READ STATUS PORT
        ANI 01H            ;MASK ALL BUT BIT 2
        JZ LOOP            ;REPEAT UNTIL BIT 2 IS HIGH
        INI                ;PUT A/D DATA INTO MEMORY
        JNZ LOOP           ;REPEAT LOOP UNTIL ALL SAMPLES
                           ;ARE TAKEN
```

RTC Polled

In the second example of polled operation the RTC is set up as a square wave rate generator. The processor tests the RTC output until it becomes true. At that time a sample may be taken under program control, a D/A may be updated, or another routine may be run. The processor then tests the RTC output until it becomes false, then resumes testing the output until it becomes true again. The processor, in this case, should continue to test the RTC until it becomes false to ensure that a service routine is not initiated at the wrong time.

```
SETUP:  MVI A,20H
        OUT CNTRL          ;SET UP CONTROL PORT SO THAT
                           ;RTC INTERRUPTS
        CALL SETRTC        ;SET UP RTC
        CALL LOADRTC       ;LOAD TIME CONSTANTS INTO RTC
LOOP:   IN STATUS          ;READ STATUS PORT
        ANI 02H            ;MASK ALL BUT RTC OUTPUT BIT
        JZ LOOP            ;REPEAT UNTIL RTC OUTPUT IS
                           ;HIGH
WORK:   DO WHATEVER IS REQUIRED WHEN THE RTC TIMES OUT
TEST:   TEST TO SEE IF LOOP HAS BEEN REPEATED ENOUGH
        TIMES. IF SO, EXIT
LOOP2:  IN STATUS          ;READ STATUS PORT
        ANI 02H            ;MASK ALL BUT RTC OUTPUT BIT
        JZ LOOP2           ;REPEAT UNTIL RTC OUTPUT IS LOW
        JMP LOOP           ;REPEAT LOOP
```

Interrupt Flag Polled

In this mode, the processor tests the interrupt flag until it becomes true. Then the flag is reset, the service routine is run, and the interrupt flag is tested again until true. Since the processor resets the flag before running the service routine, the flag can only be true when the next event occurs. The source of interrupts is determined by writing to the control port.

```
SETUP:  MVI A,INTMODE
        OUT CNTRL          ;SET UP CONTROL PORT FOR
                           ;DESIRED INTERRUPT MODE
        CALL SETRTC        ;SET UP REAL TIME CLOCK
        CALL LOADTC        ;LOAD TIME CONSTANTS INTO RTC
LOOP:   IN STATUS          ;READ THE STATUS PORT
        ANI 80H            ;MASK ALL BUT THE INTERRUPT
                           ;REQUEST FLIP-FLOP
        JZ LOOP            ;REPEAT LOOP UNTIL INTERRUPT
                           ;REQUEST FLIP-FLOP IS VALID
        OUT CNTRL          ;RESET INTERRUPT REQUEST
                           ;FLIP-FLOP
WORK:   DO WHATEVER THE ROUTINE IS SUPPOSED TO
TEST:   TEST TO SEE IF REQUIRED NUMBER OF ITERATIONS
        HAVE BEEN PERFORMED
        JMP LOOP           ;REPEAT LOOP IF NOT
```

3.6 REAL TIME CLOCK

The RTC requires a 2 MHz clock input. The clock is derived from the S-100 bus CLOCK* line. The 8253 IC has three counters, the first two of which are cascaded to form the RTC. The output of the third counter is sent to the status port and can be used as a general purpose counter. The counters have separate data ports and a common control port. The control port determines the characteristics of each counter. The data ports for counters 0, 1, and 2 are at locations 8, 9, and A, respectively, of the board address space. The control port is at location B of the board address space.

Figure 8 summarizes the configuration of the four field control word. The first field, bits D7 and D6, selects the counter to which the other three fields refer. The second field, bits D5 and D4, determines how the counters are loaded. The ADDA-8 does not allow read operations so the Counter Latching Operation of the 8253 can not be implemented on the board. The board uses the block of four addresses as an input status port for polled operation. The third field, bits D3 through D1, select the counter mode. Mode 2 is the rate generator mode. Mode 3 is a square wave generator. The fourth field, bit D0, determines whether the count proceeds in binary or BCD.

CONTROL WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	L1	L0	M2	M1	M0	BCD

DEFINITION OF CONTROL FIELDS

SC-SELECT COUNTER

SC1	SC0	
0	0	SELECT COUNTER 0
0	1	SELECT COUNTER 1
1	0	SELECT COUNTER 2
1	1	ILLEGAL

L-LOAD

L1	L0	
0	0	COUNTER LATCHING OPERATION (NOT APPLICABLE TO THIS BOARD)
1	0	LOAD MOST SIGNIFICANT BYTE ONLY
0	1	LOAD LEAST SIGNIFICANT BYTE ONLY
1	1	LOAD LEAST SIGNIFICANT BYTE FIRST, THEN MOST SIGNIFICANT BYTE

M-MODE

M2	M1	M0	
0	0	0	MODE 0
0	0	1	MODE 1
X	1	0	MODE 2
X	1	1	MODE 3
1	0	0	MODE 4
1	0	1	MODE 5

BCD

0	BINARY COUNTER 16-BITS
1	BINARY CODED DECIMAL (BCD) COUNTER (4 DECADES)

Figure 8 8253 control word

To set up the real time clock determine the time required (in microseconds) between cycles. Double the number to derive the number of clock cycles to be counted. Factor the number of clock cycles into two convenient 16-bit numbers. The 16-bit numbers are loaded into the the two counters of the RTC.

For sampling periods of up to 0.65 seconds, a convenient way to set up the RTC is to load timer 0 with 2, so that its output is 1 MHz. The second counter is loaded with the number of microseconds desired between samples.

The minimum count that can be loaded into either counter is 2. If a 1 is loaded, the output of the counter always remains high. A count of 0 is interpreted as the maximum count (65 536). The output of the first counter can be set anywhere between 1 and 32768 microseconds to provide the clock for the second counter.

Two possible routines for servicing the RTC are SetRTC and LoadTC. SetRTC loads the proper mode into counters 0 and 1. A repetitive mode is desired, so either mode 2 or mode 3 can be selected. Mode 2 is the rate generator mode. Mode 3 is a square wave generator. LoadTC loads the time constants into the two counters. Loading the time constants starts the counters.

```
SetRTC: mvi a,3EH
        out RTCSts      ;set up counter 0 as square
                        ;wave rate generator
        mvi a,7EH
        out RTCSts      ;set up counter 1 as square
                        ;wave rate generator
        ret


LoadTC: lxi h,TC0       ;put address where time
                        ;constant 0 is stored in hl
        mvi c,TC0Add    ;put address of counter 0 in c
        outi            ;move low byte of time constant
                        ;0 into time constant register
        outi            ;now move high byte
        inr c           ;now address of counter 1
                        ;is in c
        outi            ;move low byte of time constant
                        ;1 into time constant register
                        ;it is assumed that time
                        ;constant 1 is stored immediately
                        ;after time constant 0 in memory
        outi            ;now move high byte
        ret
```

4.0 THEORY OF OPERATION

This section of the ADDA-8 manual contains a detailed explanation of board operation. Figure 9 is the block diagram of the ADDA-8. The following circuits are discussed:

* Board address selection
* Control port
* Status port
* Real time clock
* Wait state generator
* Analog to digital conversion
* Digital to analog conversion
* Interrupt control

4.1 BOARD ADDRESSING AND DECODING LOGIC

The board decodes 16 memory or I/O locations. Address lines A4 through A15 are compared to the setting of switches SW1-4 through SW1-1 and SW2-1 through SW2-8, respectively, (open switch = logic ONE) by two 25LS2521 comparators (U31 and U32). Comparator U31 also has (SINP+SOUT)* as one of its inputs (from U29-1). The final comparator input selects whether the board decodes I/O or Memory addressing. Since (SINP+SOUT)* is low only when an input or output operation is performed, if the other input is set low (J6 A-B), only I/O instructions cause a board select. Conversely, if the jumper input is set high (J6 B-C), only a memory address causes a board select.

J5 selects either 8-bit or 16-bit address decoding when the board is configured for I/O addressing.

SWO*, with PDBIN, PWR*, BOARD SELECT* (from the address decoder) and A0, A1, A2, and A3, are combined to generate the required input or output commands. The command logic equations are:

```
EVEN DATA BUS ENABLE = BOARD SELECT*.pWR*
STATUS PRT ENABLE* = (BOARD SELECT.A3.A2*.PDBIN)*
A/D DATA IN ENABLE* = (BOARD SELECT.A3.A2.A1*.A0*.PDBIN)*
CONTROL WORD WRITE = BOARD SELECT.A3.A2.A1*.A0*
RTC CE* = (BOARD SELECT.A3.A2*)*
RTC WAIT ENABLE = BOARD SELECT.A3.A2*
```

where "." indicates logical AND, and "*" indicates a complement. Figure 10 is a partial schematic of the bus interface and decoding logic circuits.

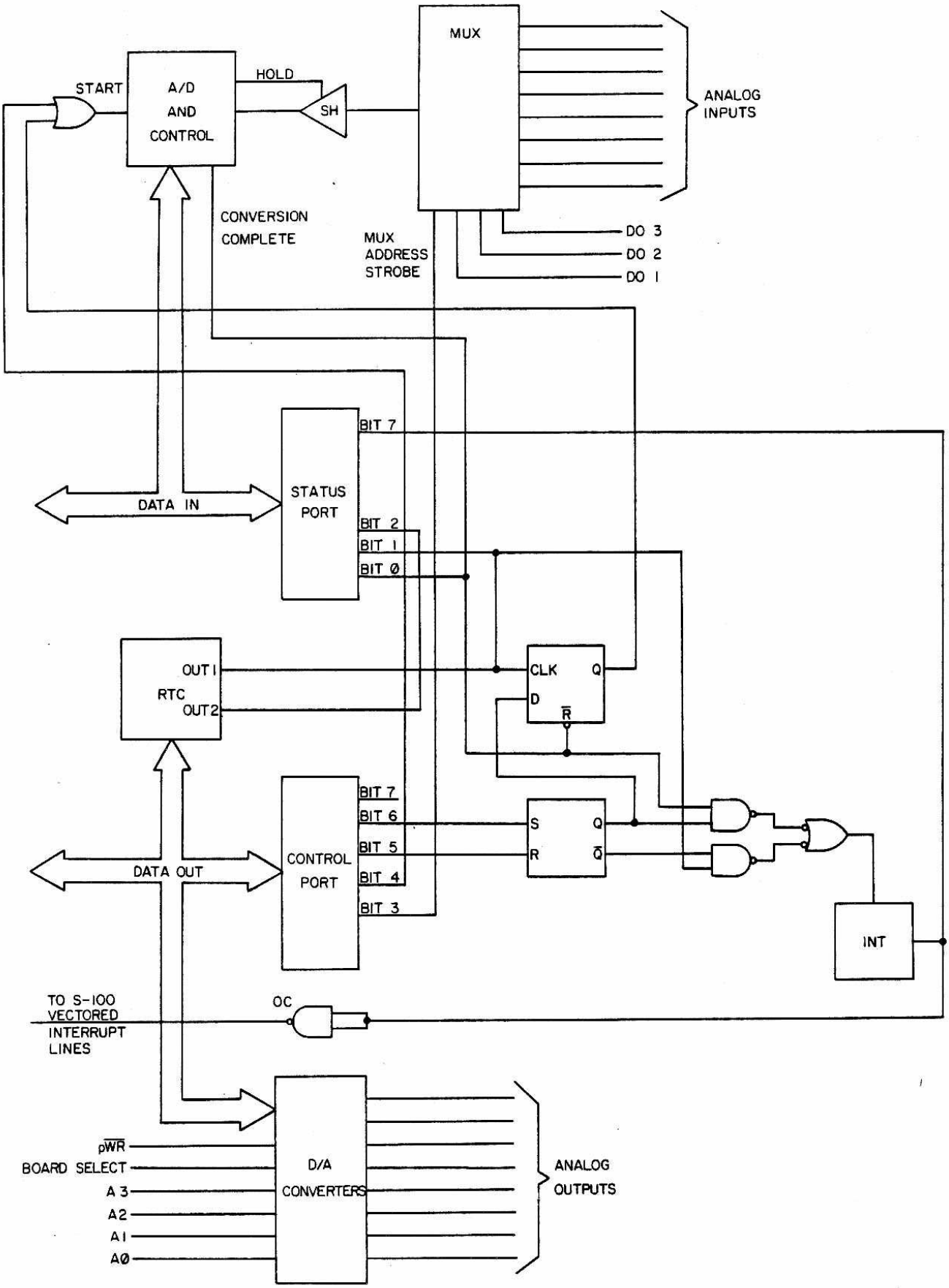


Figure 9 ADDA-8 block diagram

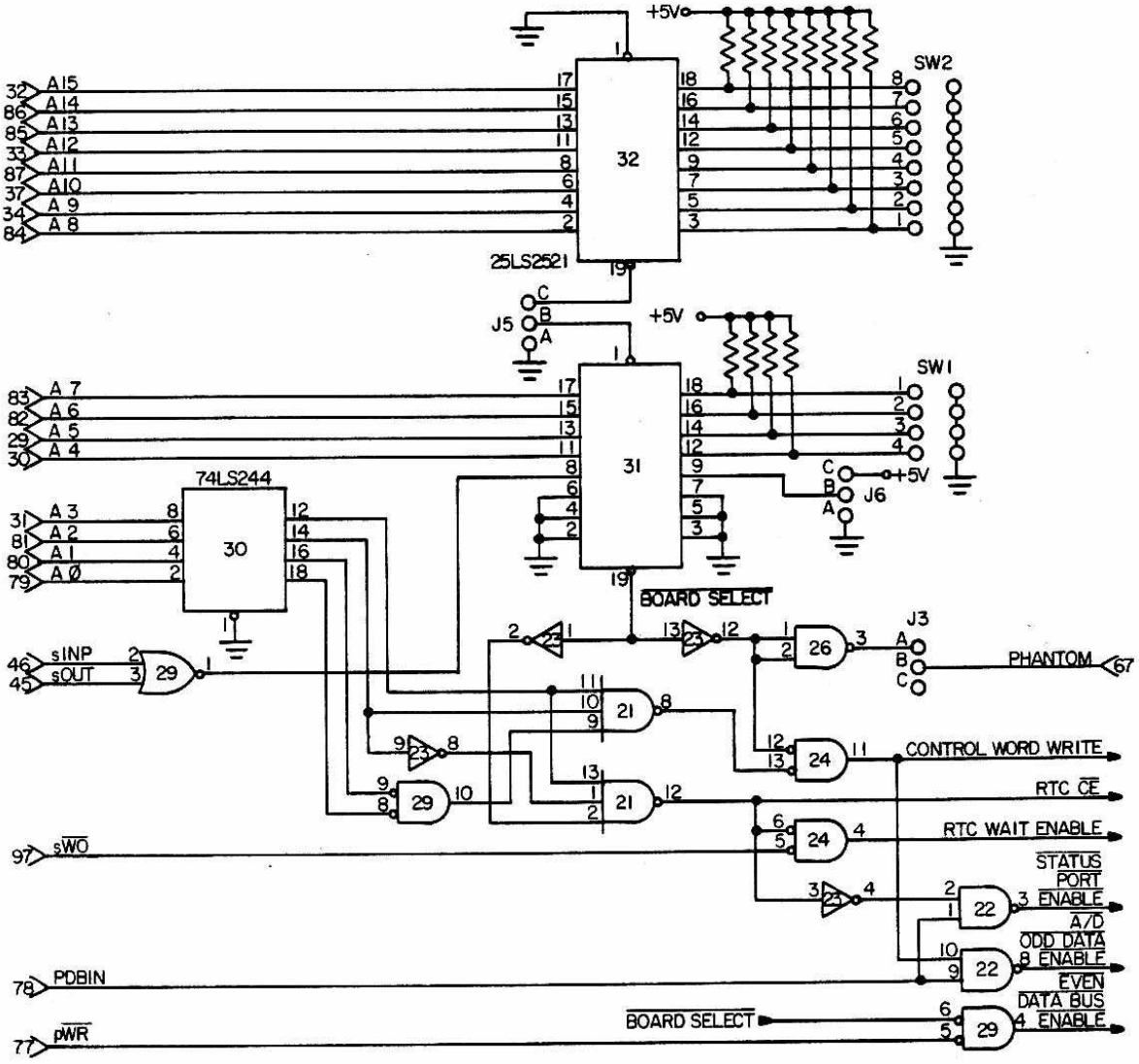


Figure 10 Bus interface and decoding logic

4.2 CONTROL AND STATUS PORTS

Control Port

The control port at location "C" of the board address space allows software to control several board functions. Figure 11 is a partial schematic of the control port circuit. When address "C" is selected, the CONTROL WRITE line (reset U5-1) goes high, allowing the rising edge of PWR* to clock data on lines ED3 through ED7 into U5 (a hex D flip-flop) When the board address is no longer selected, U5 is again reset. A set of strobes is generated and used to control board operation. The outputs of U5 are held low via the reset pin until the port is selected. U5 pin 2 clocks the MUX address latch, U15, if data line 3 is high when the port is written to. Data lines ED0, ED1, and ED2, are the MUX address latch inputs.

The control port is defined as follows:

Bit	Function
0	MUX address 0
1	MUX address 1
2	MUX address 2
3	MUX address change strobe
4	A/D conversion start strobe
5	RTC initiates interrupt, if high
6	RTC initiates A/D, A/D initiates interrupt, if high
7	Interrupt reset

NOTE: Do not write to the control port with both bit 5 and bit 6 high. An indeterminate state occurs if both the set and reset line of the RS flip-flop are enabled simultaneously.

Status Port

A status port is provided for use in polled operation. These lines may be used to obtain status in lieu of interrupts. The four lines of the status port are:

Bit	Function
0	A/D "Conversion Complete"
1	RTC output
2	8253 OUT 2 output
7	Interrupt request

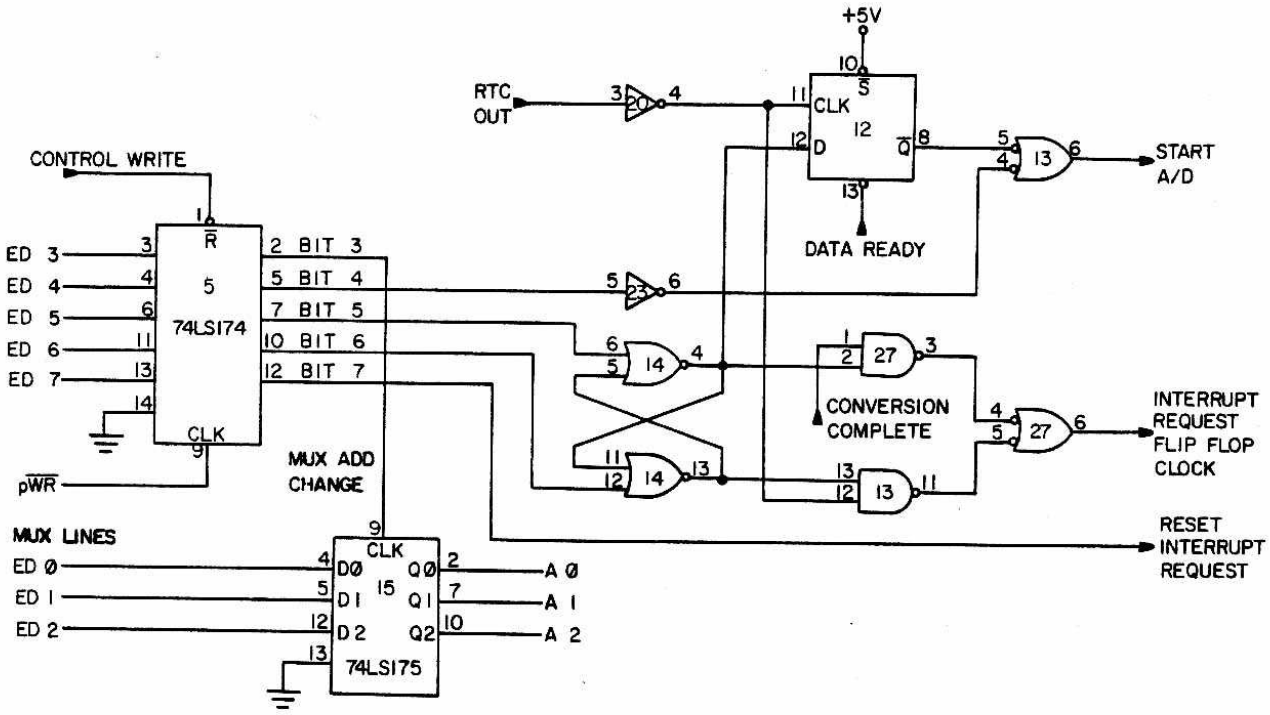


Figure 11 ADDA-8 control port

UP2-a A/D Offset Adjust trimmer
UP2-b A/D Gain Adjust trimmer
UP3 S/H Offset Adjust trimmer

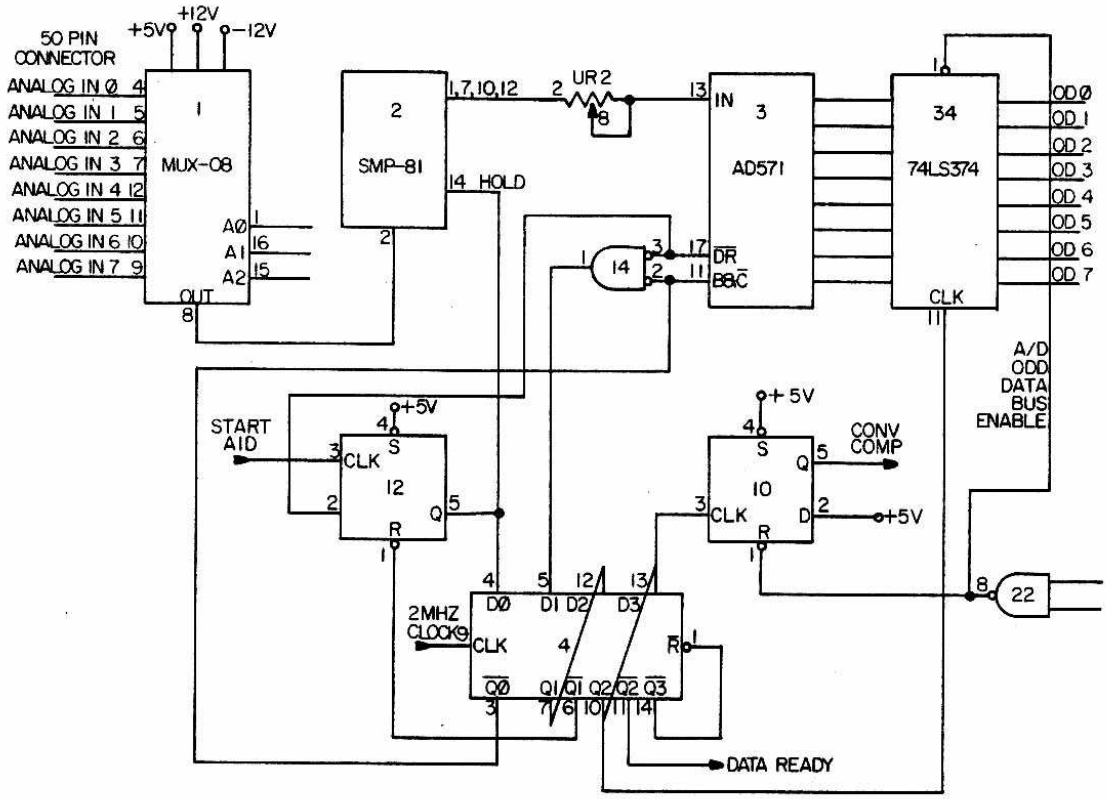


Figure 14 A/D conversion circuit

4.6 DIGITAL TO ANALOG CONVERSION

Eight separate D/A converters are used on the ADDA-8. The D/A converters are self-contained and include data latches, voltage regulators, and output voltage amplifiers on the monolithic IC. Offset and gain adjustments are provided for each converter. A 74LS138 decodes A0, A1 and A2 as addresses, and A3*, BOARD SELECT*, and PWR* as eight write strobes. The converters have a -5 volt to +5 volt output range. See Figure 15.

D/A Port - IC Correspondence

Port	IC	Trim Pot Gain	Trim Pot Offset
0	6	UP4-a	UP4-b
1	16	UP8-a	UP8-b
2	7	UP5-a	UP5-b
3	17	UP9-a	UP9-b
4	8	UP6-a	UP6-b
5	18	UP10-a	UP10-b
6	9	UP7-a	UP7-b
7	19	UP11-a	UP11-b

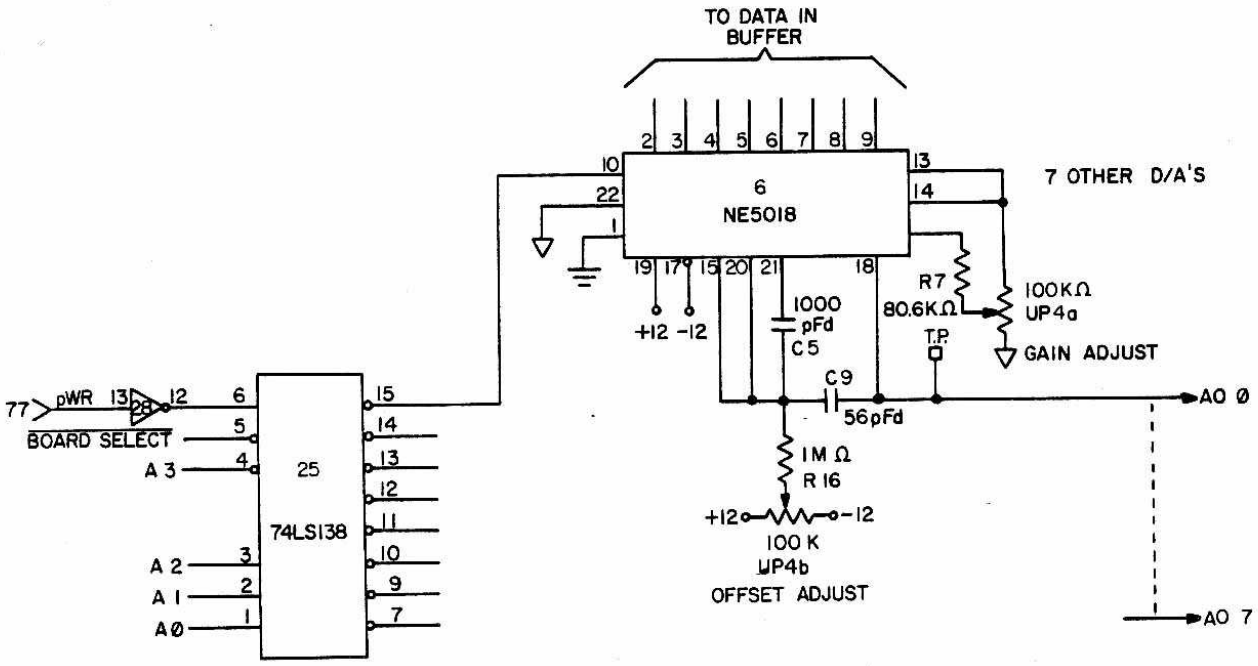


Figure 15 D/A conversion circuit

4.7 INTERRUPT CONTROLLER

Figure 16 is the partial schematic of the interrupt controller logic. An interrupt request flip-flop (U10) is clocked either by the Conversion Complete signal from the A/D, or by the RTC time out signal. The source of interrupts is selected by writing to the control port. An RS latch consisting of two cross connected NOR gates (half of U14) feeds a 2:1 data selector (half of U27, one quarter of U13) . One input to the data selector is the inverted output of the RTC; The other input is the Conversion Complete line (U10-5). A rising edge at the output of the selector clocks the interrupt request flip-flop. When clocked, the output of the flip-flop causes the open collector gate U26 to pull the selected vectored interrupt request line low.

The board can be configured so that when the processor responds to the interrupt, the request flip-flop is automatically reset. With Jumper J4 in position A-B, the request flip-flop is reset whenever the board is addressed. Alternatively, writing to the control port with bit 7 high resets the flip-flop. The S-100 reset line also clears the interrupt request flip-flop.

J1 is configured to select which vectored interrupt line is used by the interrupt request output. If interrupt driven operation of the board is not desired, the shunt at J1 is removed.

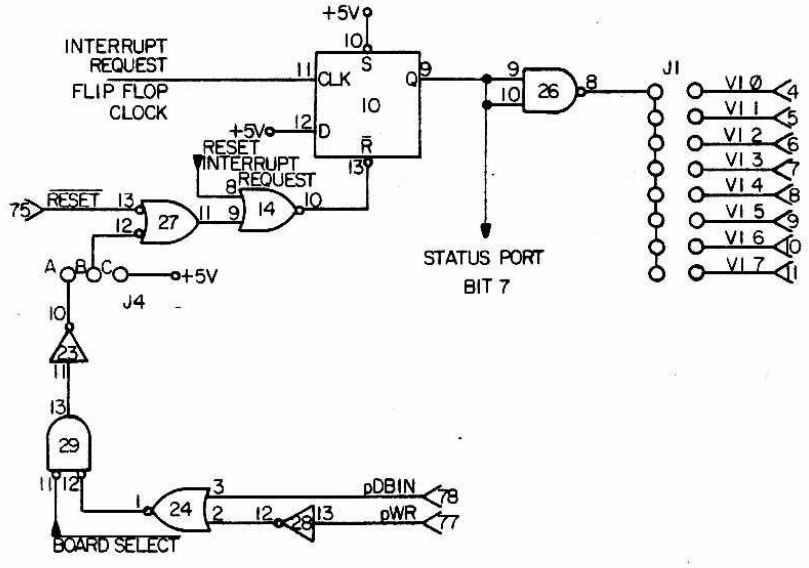


Figure 16 Interrupt controller circuit

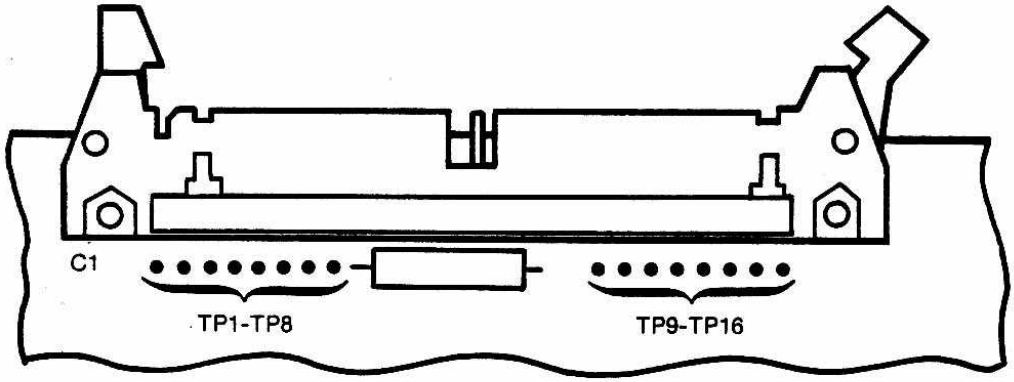
5.0 ALIGNMENT PROCEDURES

For best results, the ADDA-8 should be calibrated periodically. InterSystems provides factory alignment, or if desired the following procedures can be used.

To calibrate the ADDA-8 the following equipment is required:

* Digital Volt Meter
* Calibrated DC voltage source, with a - 5 Vdc to + 5 Vdc range, accurate to 1 mV.

Figure 17 illustrates the location of Analog In/Out test points.



TP1 Analog In 7	TP9 Analog Out 7
TP2 Analog In 6	TP10 Analog Out 6
TP3 Analog In 5	TP11 Analog Out 5
TP4 Analog In 4	TP12 Analog Out 4
TP5 Analog In 3	TP13 Analog Out 3
TP6 Analog In 2	TP14 Analog Out 2
TP7 Analog In 1	TP15 Analog Out 1
TP8 Analog In 0	TP16 Analog Out 0

Figure 17 Test point locations

5.1 D/A CALIBRATION

The following relationships exist between input codes and output voltages for the 8-bit D/A converter:

Input Code	Output Voltage
00H	-5.00 volts
80H	0.00 volts
0FFH	4.9605 volts

Since most D/A converters are not ideal, there is likely to be some deviation from these theoretical values over the lifetime of the component. The calibration procedure attempts to minimize the error at the two end points and in the middle of the range.

During the procedure, apply in succession the three input codes (00H, 80H, and 0FFH) and adjust the offset and gains trimmers as required. The component numbers given refer to A00 only. Refer to Figure 18. Each of the eight D/A channels is adjusted individually.

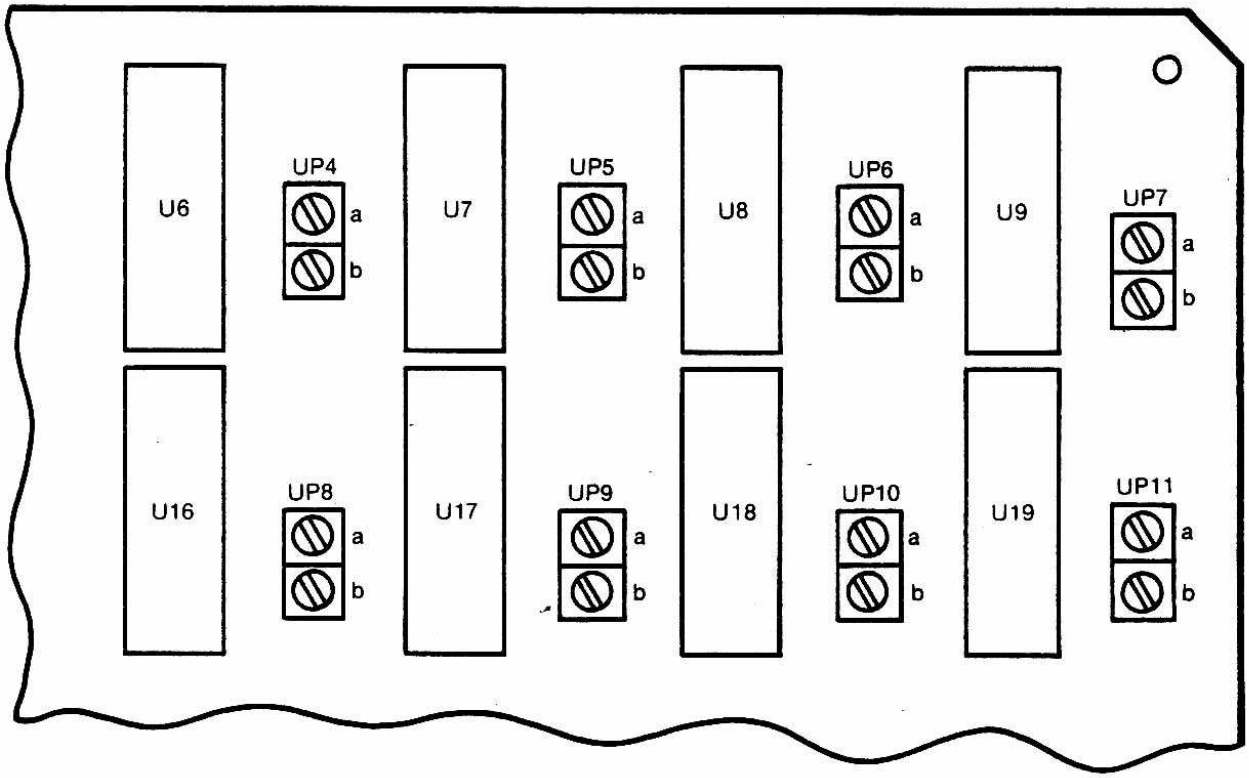


Figure 18 D/A alignment, component location

Use this procedure for D/A alignment.

1) With the input code set to 80H, adjust the offset adjust trimmer (UP4-b) until the output is approximately 0.00 volts.

2) With the input code set to 0FFH, adjust the gain adjust trimmer (UP4-a) until the output is approximately 4.9605 volts.

3) With the input code set to 00H, verify that the output is within +/- 15 millivolts of -5.00 volts.

4) Repeat the procedure starting with step 1 until all voltages deviate from ideal values by approximately the same amount (so that the total error is as small as possible).

D/A Port - IC Correspondence

Port	IC	Trim Pot	
		Gain	Offset
0	6	UP4-a	UP4-b
1	16	UP8-a	UP8-b
2	7	UP5-a	UP5-b
3	17	UP9-a	UP9-b
4	8	UP6-a	UP6-b
5	18	UP10-a	UP10-b
6	9	UP7-a	UP7-b
7	19	UP11-a	UP11-b

5.2 A/D CALIBRATION

The following relationships exist between input voltage and output code for an ideal A/D converter:

Input Voltage	Output Code
-4.9805 volts	Transition between 00H and 01H
0.01953 volts	Transition between 80H and 81H
4.9414 volts	Transition between FEH and FFH

In the following procedure, apply the three voltages listed and adjust the offset and gain trimmers so that the output code spends approximately equal time at the two codes listed for the voltages. Figure 19 shows the location of UP2 and UP3.

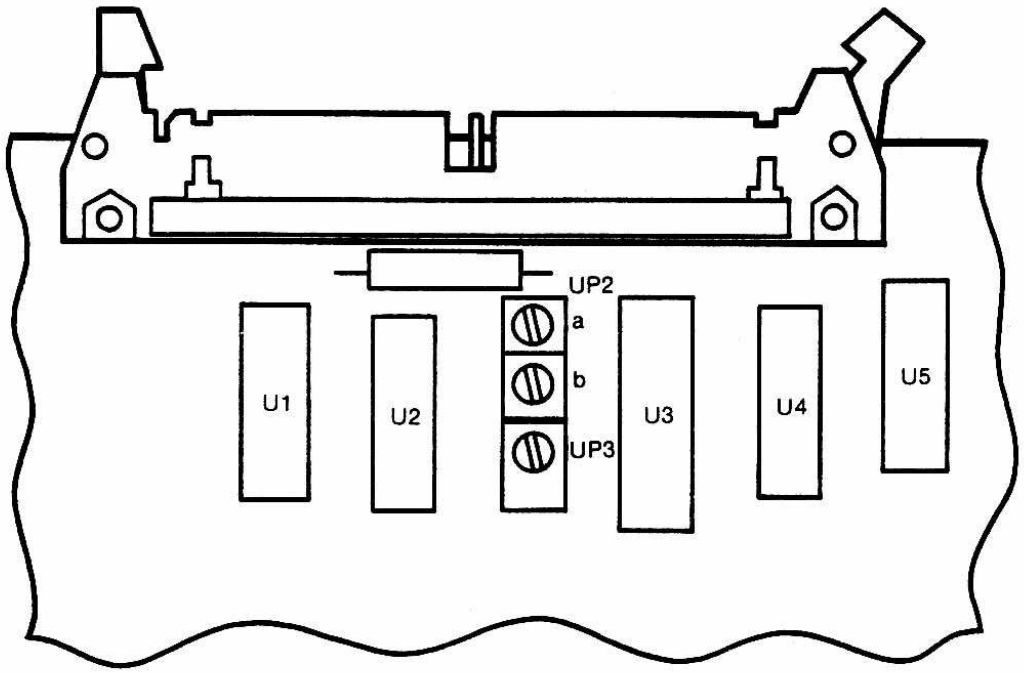


Figure 19 A/D alignment, component location

Use the following procedure to align the A/D conversion circuit.

1) Set the input channel to 0. Apply 0.00 volts to the input.

2) While the Sample/Hold (S/H) amplifier is in the sample mode, adjust the S/H offset trimmer (UP3) so that the output of the S/H amplifier is 0.00 volts.

3) Set the input voltage to 0.01953 volts. Adjust the offset trimmer (UP2-b) until the output code of the A/D flickers between 80H and 81H (at a suggested sampling rate of approximately 5 samples per second).

4) Set the input voltage to 4.9414 volts. Adjust the gain trimmer (UP2-a) until the output code of the A/D flickers between 0FEH and 0FFH.

5) Set the input voltage to -4.9805. Check that the output code flickers between 00H and 01H.

6) Repeat steps 3 through 5 to minimize error at the three input voltages.

A/D Adjustments

UP2-a	A/D Offset Adjust trimmer
UP2-b	A/D Gain Adjust trimmer
UP3	S/H Offset Adjust trimmer

6.0 PARTS LIST

INTEGRATED CIRCUITS

U1	MUX-08	U22	74LS00
U2	SMP-81	U23	74ALS04
U3	AD571JD	U24	74LS02
U4	74LS175	U25	74LS138
U5	74LS174	U26	74LS38
U6-9	NE5018	U27	74LS00
U10-12	74ALS74	U28	74LS04
U13	74LS00	U29	74ALS02
U14	74LS02	U30	74LS244
U15	74LS175	U31,32	25LS2521
U16-19	NE5018	U33	74LS373
U20	74LS04	U34	74LS374
U21	74ALS10	U35	8253

CAPACITORS

C2	4700 pf MLLRY SXK247 (4700PFD 33WVDC)
C5-8,30-33	1000 pf DG CERAMIC
C9-12,38-41	56 pf DG CERAMIC
C17,19,44,46,51	10 uf TANTALUM 35 WVDC
All others	.1 uf CERAMIC

RESISTORS AND RESISTOR NETWORKS

R1	4.75 K OHM 1% 1/4W METAL FILM
R2	10.0 OHM 1% 1/4W METAL FILM
R3-6,11-14	1.0 M OHM 1% 1/4W METAL FILM
R7-10,15-18	80.6 K OHM 1% 1/4W METAL FILM
UR1,2	9 PIN 8R SIP CSP09G-01-472

TRIMMERS

UP2	100/10 K	8P DP 7102B-213-101
UP3	100K/100K	6P DP 7108A-101-104
UP4-11	100K/100K	8P DP 7102B-210-104

REGULATORS

Q1	7812
Q2	78L05
Q3	7912
Q4	7805

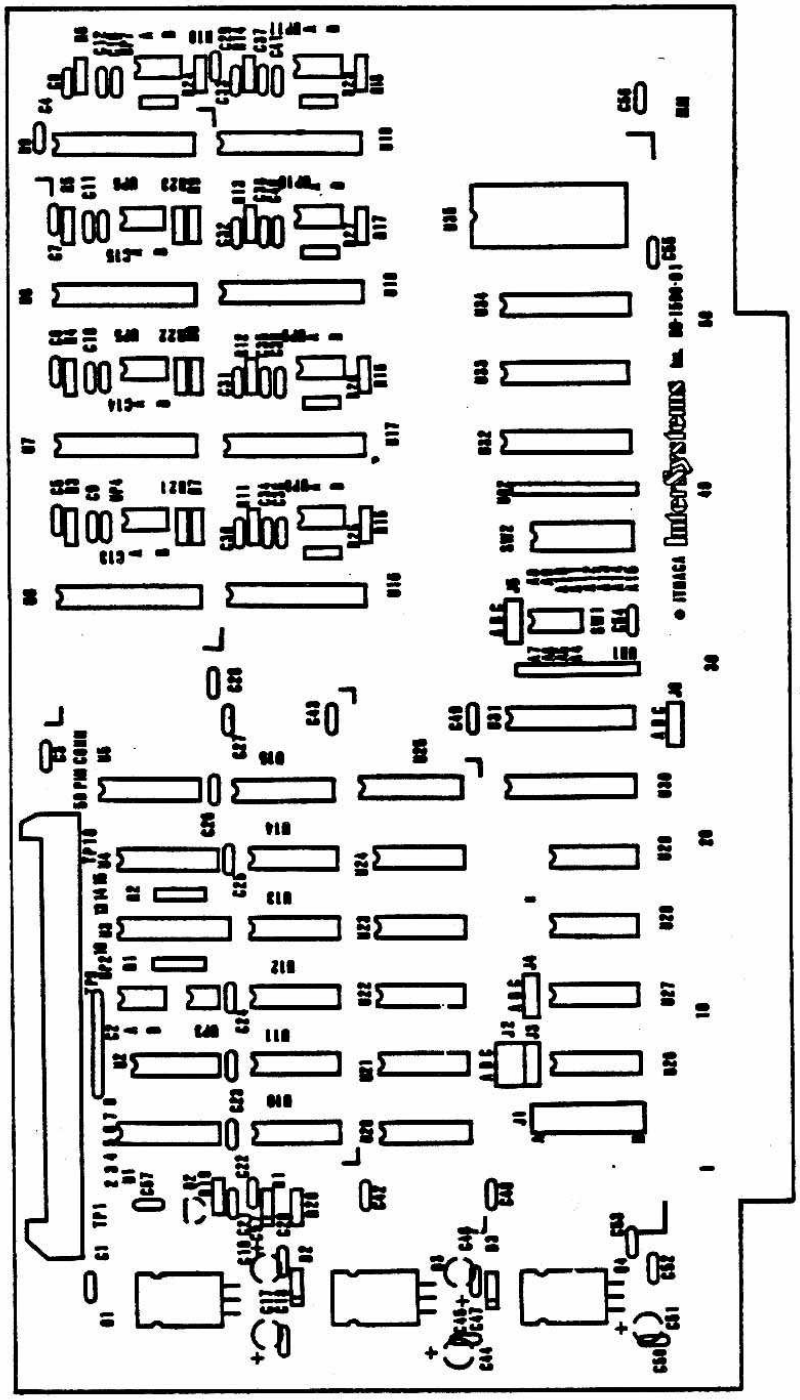
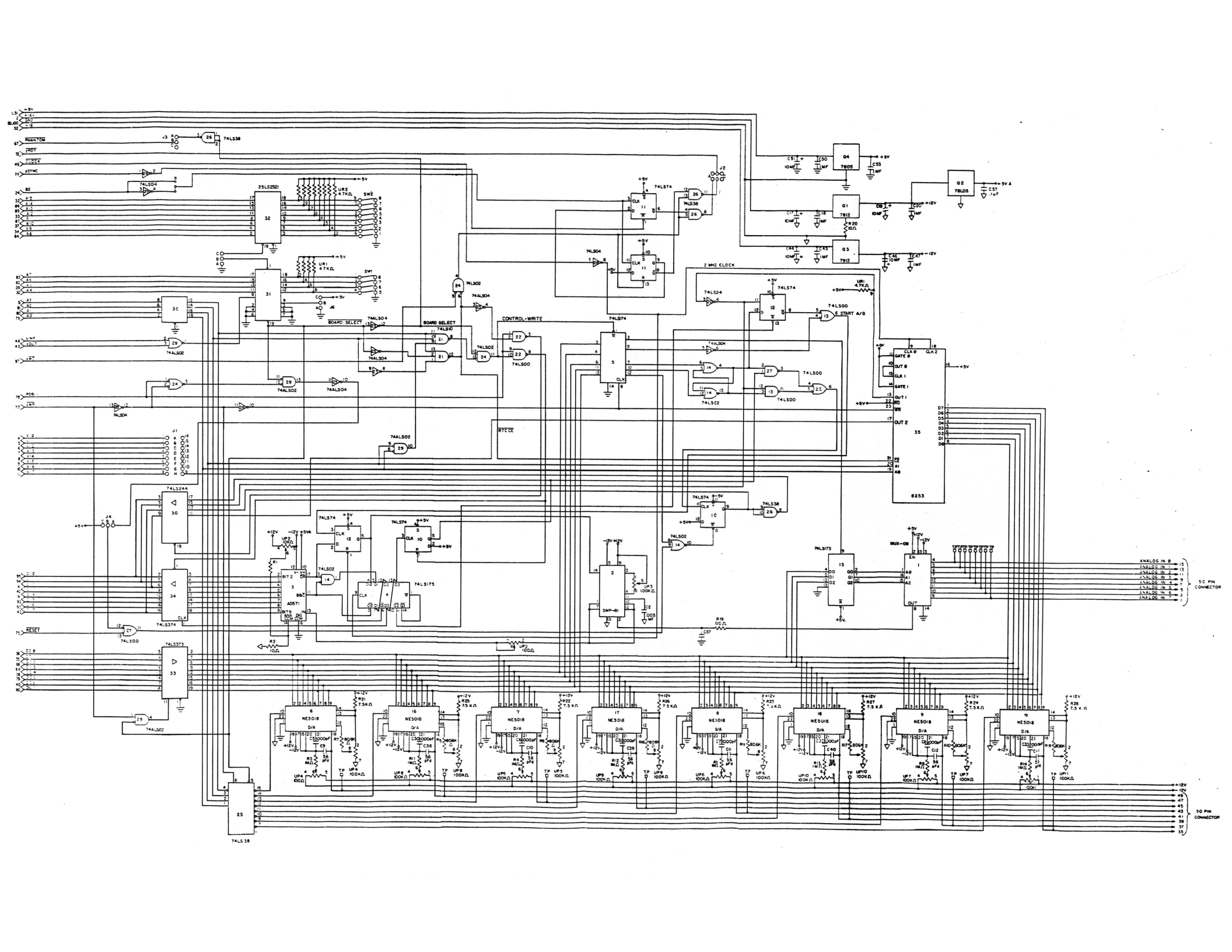


Figure 20 ADDA-8 board


PHANTOM
PSYNC
CLOCK
RESET
BOARD SELECT
CONTROL-WRITE
2 MHZ CLOCK
RTC CE
74LS38
74LS244
74LS374
74LS373
74LS175
74LS574
74LS74
74LS04
74LS02
74LS00
74LS10
74LS38
25LS2521
AD571
NE5018
8253
7805
7812
7912
78L05
6 START A/D
MUX-08
ANALOG IN 0
ANALOG IN 1
ANALOG IN 2
ANALOG IN 3
ANALOG IN 4
ANALOG IN 5
ANALOG IN 6
ANALOG IN 7
50 PIN CONNECTOR
50 PIN CONNECTOR