OMNI256 Board

256k Static Ram for IEEE-696/S-100

Technical Reference Manual

August 1985

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1.0 INTRODUCTION

This manual contains the information necessary to install and operate the OMNI256 256k static ram board in an IEEE 696 environment. In addition non-standard applications and operational theory are discussed. The OMNI256 can be used under CP/M 2.2, CP/M 3.0 (CP/M+), CP/M-86, MP/M-80, MS-DOS, CCP/M (Concurrent PC-DOS), or MP/M-86.

Fulcrum Computer Products' OMNI265 board utilizes the latest in CMOS SRAM technology to provide 256 kilobytes of fast, fully static memory for IEEE-696 S-100 computer systems. This board automatically configures to 8-bit and 16-bit service requests by the host processor. Extended 24-bit addressing is supported. All assembled boards are completely factory tested.

1.1. Hardware Features

The OMNI256 offers the following features:

1. Conforms to IEEE 696 standard. (S100 buss)

2. The memory can be located on any 256k boundary, and comes factory set as the first 256k in your system.

3. Supports 24 bit extended addressing

4. The board is fully compatible with 8-bit and 16-bit data transfers, and adjusts itself dynamically.

5. No special considerations are required for DMA (TMA) operation due to completely static design.

6. Standard OMNI256 boards support 8mhz operation populated with 120ns(-12) low power(LP) parts.

7. Board can be phantomed with pin 67 (PHANTOM*)

8. Typical Board operating power consumption of 4 watts.

9. Battery backup power down mode requires less than 50ua

2. BOARD OVERVIEW

The OMNI256 board uses a 256k linear address space starting at the base address specified by SW1. Jumpers 1 and 2 select read/write generation mode, and Jumper area B select the battery backup mode.

2.1 Factory Settings

Most of the jumpers present on the OMNI256 are strapped by means of traces on the P.C. board itself. Factory addressed to 00000h. It is set up to use system generated MWRT for write, sMEMR for read. This simplifies installation in a standard system. The following describes what options are available via jumpering/switch settings.

2.2. Address Switch Settings

The base address switch (SW1) located on the lower left of the board, just right of the 5 volt regulator circuit. SW1.3-8 correspond to address lines A18-A23. A closed switch indicates a match on a low address line. All possible setting are listed in table 2-2, below.

Table 2-2: Switch (SW1) settings for various base addresses

Address space occupancy first used	last used	switch settings SW.3	SW.4	SW.5	SW.6	SW.7	SW.8
000000h	03ffffh	ON	ON	ON	ON	ON	ON
040000h	07ffffh	OFF	ON	ON	ON	ON	ON
080000h	0Bffffh	ON	OFF	ON	ON	ON	ON
0C0000h	0fffffh	OFF	OFF	ON	ON	ON	ON
100000h	13ffffh	ON	ON	OFF	ON	ON	ON
140000h	17ffffh	OFF	ON	OFF	ON	ON	ON
180000h	1Bffffh	ON	OFF	OFF	ON	ON	ON
1C0000h	1fffffh	OFF	OFF	OFF	ON	ON	ON
200000h	23ffffh	ON	ON	ON	OFF	ON	ON
240000h	27ffffh	OFF	ON	ON	OFF	ON	ON
280000h	2Bffffh	ON	OFF	ON	OFF	ON	ON
2C0000h	2fffffh	OFF	OFF	ON	OFF	ON	ON
300000h	33ffffh	ON	ON	OFF	OFF	ON	ON
340000h	37ffffh	OFF	ON	OFF	OFF	ON	ON
380000h	3Bffffh	ON	OFF	OFF	OFF	ON	ON
3C0000h	3fffffh	OFF	OFF	OFF	OFF	ON	ON
400000h	43ffffh	ON	ON	ON	ON	OFF	ON
440000h	47ffffh	OFF	ON	ON	ON	OFF	ON
480000h	4Bffffh	ON	OFF	ON	ON	OFF	ON
4C0000h	4fffffh	OFF	OFF	ON	ON	OFF	ON

500000h	---	53ffffh	ON	ON	OFF	ON	OFF	ON
540000h	---	57ffffh	OFF	ON	OFF	ON	OFF	ON
580000h	---	5Bffffh	ON	OFF	OFF	ON	OFF	ON
5C0000h	---	5fffffh	OFF	OFF	OFF	ON	OFF	ON
600000h	---	63ffffh	ON	ON	ON	OFF	OFF	ON
640000h	---	67ffffh	OFF	ON	ON	OFF	OFF	ON
680000h	---	6Bffffh	ON	OFF	ON	OFF	OFF	ON
6C0000h	---	6fffffh	OFF	OFF	ON	OFF	OFF	ON
700000h	---	73ffffh	ON	ON	OFF	OFF	OFF	ON
740000h	---	77ffffh	OFF	ON	OFF	OFF	OFF	ON
780000h	---	7Bffffh	ON	OFF	OFF	OFF	OFF	ON
7C0000h	---	7fffffh	OFF	OFF	OFF	OFF	OFF	ON
800000h	---	83ffffh	ON	ON	ON	ON	ON	OFF
840000h	---	87ffffh	OFF	ON	ON	ON	ON	OFF
880000h	---	8Bffffh	ON	OFF	ON	ON	ON	OFF
8C0000h	---	8fffffh	OFF	OFF	ON	ON	ON	OFF
900000h	---	93ffffh	ON	ON	OFF	ON	ON	OFF
940000h	---	97ffffh	OFF	ON	OFF	ON	ON	OFF
980000h	---	9Bffffh	ON	OFF	OFF	ON	ON	OFF
9C0000h	---	9fffffh	OFF	OFF	OFF	ON	ON	OFF
A00000h	---	A3ffffh	ON	ON	ON	OFF	ON	OFF
A40000h	---	A7ffffh	OFF	ON	ON	OFF	ON	OFF
A80000h	---	ABffffh	ON	OFF	ON	OFF	ON	OFF
AC0000h	---	Afffffh	OFF	OFF	ON	OFF	ON	OFF
B00000h	---	B3ffffh	ON	ON	OFF	OFF	ON	OFF
B40000h	---	B7ffffh	OFF	ON	OFF	OFF	ON	OFF
B80000h	---	BBffffh	ON	OFF	OFF	OFF	ON	OFF
BC0000h	---	Bfffffh	OFF	OFF	OFF	OFF	ON	OFF
C00000h	---	C3ffffh	ON	ON	ON	ON	OFF	OFF
C40000h	---	C7ffffh	OFF	ON	ON	ON	OFF	OFF
C80000h	---	CBffffh	ON	OFF	ON	ON	OFF	OFF
CC0000h	---	Cfffffh	OFF	OFF	ON	ON	OFF	OFF
D00000h	---	D3ffffh	ON	ON	OFF	ON	OFF	OFF
D40000h	---	D7ffffh	OFF	ON	OFF	ON	OFF	OFF
D80000h	---	DBffffh	ON	OFF	OFF	ON	OFF	OFF
DC0000h	---	Dfffffh	OFF	OFF	OFF	ON	OFF	OFF
E00000h	---	E3ffffh	ON	ON	ON	OFF	OFF	OFF
E40000h	---	E7ffffh	OFF	ON	ON	OFF	OFF	OFF
E80000h	---	EBffffh	ON	OFF	ON	OFF	OFF	OFF
EC0000h	---	Efffffh	OFF	OFF	ON	OFF	OFF	OFF
F00000h	---	F3ffffh	ON	ON	OFF	OFF	OFF	OFF
F40000h	---	F7ffffh	OFF	ON	OFF	OFF	OFF	OFF
F80000h	---	FBffffh	ON	OFF	OFF	OFF	OFF	OFF
FC0000h	---	FFFFFFh	OFF	OFF	OFF	OFF	OFF	OFF

2.3. Jumper Settings

There are 3 jumper areas on the OMNI256. Description/usage of each follows. Refer to APPENDIX C for help in locating, if needed.

2.3.1. Battery Backup Options

This section refers to jumper area 'B', located on the left lower corner of the OMNI256. It has six pins, numbered from left to right as 1-6. Shunt pins 1-2 if not using battery backup, otherwise leave open and jumper the other pins as follows:

Jumper 5-6 is for trickle charging your battery. Shunt if using a chargeable battery. Warning: Do not shunt this if the battery type you are using is non chargeable, i.e lithium or alkaline.

Pins 3-4 connect to the battery. Pin 3 connects to the (-) negative end of battery. Pin 4 is the positive connection.

Refer to the theory of operation for consideration of various battery types.

2.3.2. J1 - MWRT generation

This jumper is located near the edge connector just left of the silk screened marking for S100 buss pin 20. It is used to configure the board to use either system generated MWRT or to generate MWRT from sOUT and pWR for local use. To use system MWRT shunt pins 1-3 on J1. For board generated MWRT shunt pins 1-2. Board generation of MWRT does not affect system MWRT signal. This jumper is factory configured for system MWRT use. If a change is necessary then a trace may need to be cut on the solder side of the board. This is primarily intended for systems that do not generate MWRT.

2.3.3. J2 - sMEMR or pDBIN data reads

This jumper is located near the edge connector just right of the silk screened marking for S100 buss pin 20. It is used to configure determine what signal the OMNI256 is to use for write generation.

2.4. EPROM COMPATIBILITY

The pinout of the HM 6264 LP -12 is pin-for-pin compatible for use with industry standard 2764 type EPROM devices. Due to the OMNI256 compatibility with 16-bit wide data transfers, odd and even memory locations are stored in to physically different devices. Due to this pairing requirement, the minimum ROM area is 16k bytes. i.e. two 2764's occupying two socket positions. For placement/ address decoding considerations, check section 5.4. Power and speed considerations may apply depending on device type utilized.

2.5. EEPROM Compatibility

There are several EEPROM devices available that latch addresses and data for writing (i.e X2864A by Xicor), and therefore could potentially be utilized. Power and speed considerations apply.

2.6. DMA (TMA) Considerations

This card does not have restrictions as to the length of a DMA operation, since it is static by design.

2.7. PHANTOM* usage

This card is not selectable on assertion of PHANTOM*. This is used primarily for booting purposes. For example, a disk controller may need to have a boot prom resident in the memory image that is also occupied by the OMNI256. The conflict is resolved by the disk controllers' assertion of PHANTOM*, and forcing the OMNI256 to deselect.

3.0 BOARD INSTALLATION

This portion of the manual provides instructions for preparing and installing your OMNI256. Unpacking and inspection instructions are included, as are instructions for setting up the jumper and switch options.

3.1 Unpacking and Inspection

All computer cards must be handled with care, since the components on them may be damaged by bending or bumping. Also the chips may come loose if the board is mishandled.

You should be especially careful of static electricity when you handle the OMNI256 board, since the memory chips are of CMOS technology and susceptible to damage from static. Discharge any static that has built up on your body by touching an electrically grounded piece of metal (such as other grounded equipment, or a metal desk) before handling the board. For added safety keep the board in its' conductive envelope during transportation or handling.

Upon receipt of your OMNI256, immediately inspect the shipping carton and the board itself for evidence of mishandling or damage during transit. If the shipping container is severly damaged or waterstained, contact the carrier and request that his agent be present when any additional cartons are opened. If the carton is opened and the carrier's agent is not present, save the carton and all shipping materials for the agent's inspection.

The shipping carton and packing material have been carefully designed to protect the OMNI256 during shipment. If it becomes necessary to return a board, it should be repacked in its original shipping carton with its original packing material.

Check that all chips are seated in their sockets. If a chip is not fully seated in its socket, be sure that all of the pins of the chip are above the holes in its socket. Push gently on the end that is sticking up from the board until the chip is evenly flat against the socket.

Also, be sure that the black rectangular jumpers connectors that stand above the board are pushed all the way down on their jumper pins. If any of the jumpers have fallen off the board, read the next section and replace them on the correct pins.

3.2. Seating the Board

Once you are certain that the jumpers are set correctly, install the board in your system. Make sure that the computer is not plugged on. Do not install or handle this board with the system on, as this may cause damage to the board components, traces, and other boards in your system.

Slide the board in any free slot on the motherboard, making sure the component side is oriented correctly. Gently push the top of the board until the board is seated in the motherboard.

If you need to remove the board, pull gently on the top of board and rock it to loosen it from the edge connector, then simply pull up.

4. MAINTENANCE

Once past burn-in it is unlikely that this card will require any maintenance. If your computer system reports that there is a bad byte of RAM on the board, use the table 4-5 to determine which chip may be the culprit.

Table 4-5

RAM select map

CCCCC	BBBBBB	AAAAAA	
Even UC01 +20000 to 23FFF	Even UB01 +24000 to 27FFF	Even UA01 +28000 to 2BFFF	1
Even UC02 +2C000 to 2FFFF	Even UB02 +3C000 to 3FFFF	Even UA02 +34000 to 37FFF	2
	Even UB03 +30000 to 33FFF	Even UA03 +34000 to 37FFF	3
	Even UB04 +1C000 to 1FFFF	Even UA04 +0C000 to 0FFFF	4
	Even UB05 +00000 to 03FFF	Odd UA05 +28000 to 2BFFF	5
	Even UB06 +04000 to 07FFF	Odd UA06 +24000 to 27FFF	6
	Even UB07 +08000 to 0BFFF	Odd UA07 +20000 to 23FFF	7
	Even UB08 +18000 to 1BFFF	Odd UA08 +3C000 to 3FFFF	8
	Even UB09 +14000 to 17FFF	Odd UA09 +38000 to 3BFFF	9
	Even UB10 +10000 to 13FFF	Odd UA10 +30000 to 33FFF	10
	Odd UB11 +2C000 to 2FFFF	Odd UA11 +34000 to 37FFF	11
	Odd UB12 +10000 to 13FFF	Odd UA12 +18000 to 1BFFF	12
Odd UC13 +08000 to 0BFFF	Odd UB13 +14000 to 17FFF	Odd UA13 +1C000 to 1FFFF	13
Odd UC14 +0C000 to 0FFFF	Odd UB14 +04000 to 07FFF	Odd UA14 +00000 to 03FFF	13

5. THEORY OF OPERATION

The OMNI256 memory board conforms to the IEEE-696/ S-100 standards for memory devices. This section assumes that the reader has some experience in logic circuitry.

Because the OMNI256 is a static memory which does not require refresh cycles to preserve the contents of memory, its operation is somewhat simple and straightforward.

5.1 Board select generation

U3, an 8-bit comparator is used to generate BDSEL* an active low signal indicating that the address on the host buss is within the memory reserved for this board, and that we are not doing an IO cycle. PHANT*, SINTA* also prevent BDSEL* activation from U3. If the board is selected (BDSEL*) then SIXTN is forced high, indicating that we are capable of 16-bit transfer, the state rom (U15) is activated, along with U1-2, U12-13 , the ram select drivers. If PHANTOM* is low (active) then BDSEL* will not occur.

5.2 Address buffering

The address lines A0-A15 (16 lines) are buffered through schmitt trigger type buffers (U7, U8) to drive the ram array. A16 is buffered through U4, this selects which pair of 138's will be active.

5.3. 8-bit/16-bit bus operation

The OMNI256 has two internal data paths or busses. All of the memory chips which are addressed when A0 is true are connected to one bus (ODD bus), while those chips which are addressed when A0 is false are connected to another bus (EVEN bus).

A bipolar PROM, U15, generates from A0, sXTRQ (16-bit data transfer request from host), and sMEMR the proper logical arrangement of the ODD/EVEN data paths.

U10 acts as a multiplexor for the odd/even busses converging their output to DO0-7. For even 8-bit reads, the data flows through from the even ram array do cross-link buffer U9 (74LS245) and out to the host. Odd 8-bit read is similar; The data flows from the odd data path through buffer U10 (74LS244) and then out to the system buss.

For an 8-bit write operation U11 (74LS245) buffers the data incoming from the system buss, and this is channeled to either the even bank, if U10 (74LS244) ~~is~~ enabled, or the odd bank if U10 is not enabled.

For 16-bit bus operation the cross-link buffer U10 is remains disabled for both reads and writes. The Odd data is buffered by U11 (74LS245) to/from the ODD data buss. The even data is buffered by U9 (74LS245) to/from the EVEN data buss. This occurs simultaneously for 16-bit operation.

The proper select/direction signals are generated by U15 (TBP18S030) depending on the current state of the host buss. Bus contention glitches are avoided by enabling the S-100 bus buffers U9 and U11 only after the internal bus connections have been established. This is possible because sMEMR which determines whether or not the cycle is to a read or a write is established before pDBIN/MWRT is asserted.

5.4. RAM select routing

The address lines A17*, A16*, A14, A15, along with the four select lines (SEL0-3) generated by U15, and BDSEL* are routed to the RAM select decoders U1, U2, U12, and U13. This maps the memory devices as per table 4-5.

5.5. Battery backup operation

Battery backup operation is convened through the use of low power CMOS static ram, and some simple circuitry. During normal power operation the R5-D4 junction is at 4.3v which biases Q1 into a conducting region, and thereby the collector is at a logic high equivalent. This drives pin 26, common to all rams, high.

When a power drop (power failure or normal shutdown) occurs Q1 no longer conducts, and pin 26 is pulled low by R2. This signals the rams to go into power-down mode.

Further, diode D3 prevents the backup battery from powering anything but the ram chips on power down. Diode D1 is used to prevent the battery from charging from the logic supply. If pins 5-6 are shunted then the battery is charged through R4 and D2 from the logic supply. Diode D3 is a hot carrier type to reduce forward voltage drop to a few millivolts.

5.6 Backup Battery Selection

There are quite a few choices for the type of backup battery. We suggest the use of lithium. It requires no charging, and is low maintenance. NiCd may be used, but the time between power ons is seriously compromised. This is due to a loss of 1%/day of NiCd charge. A minimum of three NiCd cells are required to meet the minimum backup voltage requirement of 3 volts (3 * 1.2 = 3.6). Other candidates include Gel Cell and Alkaline. Alkaline batteries are not as long lasting as Lithium-Manganese Oxide systems, but they are much cheaper. Use of higher voltages increases power requirements and may shorten battery life.

6.0 ENGINEERING SPECIFICATIONS

6.1 PHYSICAL CHARACTERISTICS

The OMNI256 is a single height card that occupies one card position in an S100 motherboard.

6.2 ENVIRONMENTAL CHARACTERISTICS

Temperature:

Operating	0 C to +50 C
Non-operating	-50 C to +85 C

Humidity:

Operating: up to 90% relative humidity without condensation.

Non-operating: all conditions without condensation or frost.

6.3 DC Power Requirements

operating characteristics

+8 volts

500ma maximum

battery backup mode characteristics

+3.0 volts

50ua maximum

10ua typical

6.4 - IEEE 696/ S100 specifications

All signals are TTL level except where noted and follow the usual convention of a low voltage being 0 or FALSE and a high voltage being a 1 or TRUE. Signals that are active low follow the opposite convention and are denoted by the * suffix. Inputs For complete timing specifications refer to the IEEE-696 standard document: Standard specifications for S100 bus interface devices IEEE task 696.1/ D2.

Pin NO.	Signal Mnemonic	Description
1	+8 Volts	Instantaneous minimum greater than 7 volts Instantaneous maximum less than 25 volts Average maximum less than 11 volts
4	VI0*	Vectored interrupt line 0.
5	VI1*	Vectored interrupt line 1.
6	VI2*	Vectored interrupt line 2.
7	VI3*	Vectored interrupt line 3.
8	VI4*	Vectored interrupt line 4.
9	VI5*	Vectored interrupt line 5.
10	VI6*	Vectored interrupt line 6.
11	VI7*	Vectored interrupt line 7.
12	NMI*	Non-maskable interrupt.
15	A18	Extended address bit 18
16	A16	Extended address bit 16
17	A17	Extended address bit 17
24	Φ	The master timing signal for the bus.
29	A5	Address bit 5
30	A4	Address bit 4
31	A3	Address bit 3

32	A15	Address bit 15
33	A12	Address bit 12
34	A9	Address bit 9
35	DO1/DATA1	Data out bit 1, bidirectional data bit 1
36	DO0/DATA0	Data out bit 0, bidirectional data bit 0
37	A10	Address bit 10
38	DO4/DATA4	Data out bit 4, bidirectional data bit 4
39	DO5/DATA5	Data out bit 5, bidirectional data bit 5
40	DO6/DATA6	Data out bit 6, bidirectional data bit 6
41	DI2/DATA10	Data in bit 2, bidirectional data bit 10
42	DI3/DATA11	Data in bit 3, bidirectional data bit 11
43	DI7/DATA15	Data in bit 7, bidirectional data bit 15
44	sM1	The status signal which indicates that the current cycle is an op-code fetch.
45	sOUT	The status signal identifying the data transfer bus cycle to an output device.
46	sINP	The status signal identifying the data transfer bus cycle from an input device.
47	sMEMR	The status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycle(s)
48	sHLDA	The status signal which acknowledges that a HALT instruction has been executed.
50	GND	Common with pin 100.
51	+8 volts	Common with pin 1.
54	SLAVE CLR*	A reset signal to reset bus slaves. Must be active with POC* and may also be generated by external means.
50	GND	Electrical ground

58	sXTRQ	The status which requests 16-bit slaves to assert SIXTN*
59	A19	Extended Address bit 19
60	SIXTN*	The signal generated by 16-bit slaves in response to the 16-bit request signal sXTRQ*.
61	A20	Extended Address bit 20
62	A21	Extended Address bit 21
63	A22	Extended Address bit 22
64	A23	Extended Address bit 23
67	PHANTOM*	A bus signal which disables slave devices and enables phantom slaves - primarily used for bootstrapping systems without hardware front panels.
68	MWRT	pWR* - sOUT
73	INT*	The primary interrupt request bus signal.
77	pWR	The control signal signifying the presence of valid data on DO or DATA bus
78	pDBIN	The control signal that requests data on the DI bus or DATA bus from the currently addressed slave.
79	A0	Address bit 0
80	A1	Address bit 1
81	A2	Address bit 2
82	A6	Address bit 6
83	A7	Address bit 7
84	A8	Address bit 8
85	A13	Address bit 13
86	A14	Address bit 14
87	A15	Address bit 15
88	DO2/DATA2	Data out bit 2, bidirectional data bit 2
89	DO3/DATA3	Data out bit 3, bidirectional data bit 3

90	DO7/DATA7	Data out bit 7, bidirectional data bit 7
91	DI4/DATA4	Data in bit 4, bidirectional data bit 4
92	DI5/DATA5	Data in bit 5, bidirectional data bit 5
93	DI6/DATA6	Data in bit 6, bidirectional data bit 6
94	DI1/DATA1	Data in bit 1, bidirectional data bit 1
95	DI0/DATA0	Data in bit 0, bidirectional data bit 0
96	sINTA	The status signal identifying the bus input cycle(s) that may follow an accepted interrupt request presented on INT*.
97	sWO*	The status signal identifying a bus cycle which transfers data from a bus master to a slave.
99	POC*	The power-on clear signal for all bus devices
100	GND	System electrical ground.

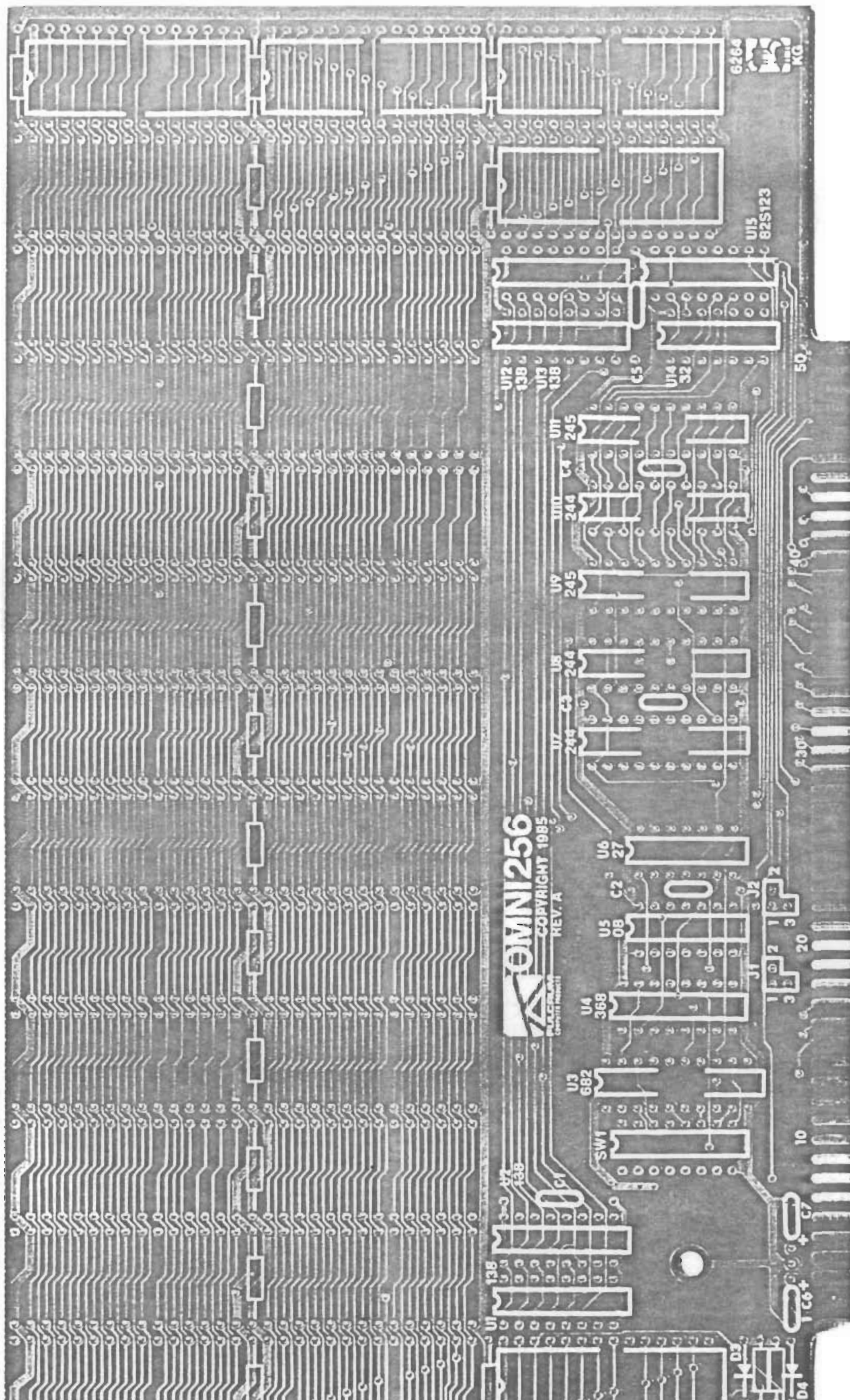
APPENDIX B: State PROM table for 74LS244 buffers

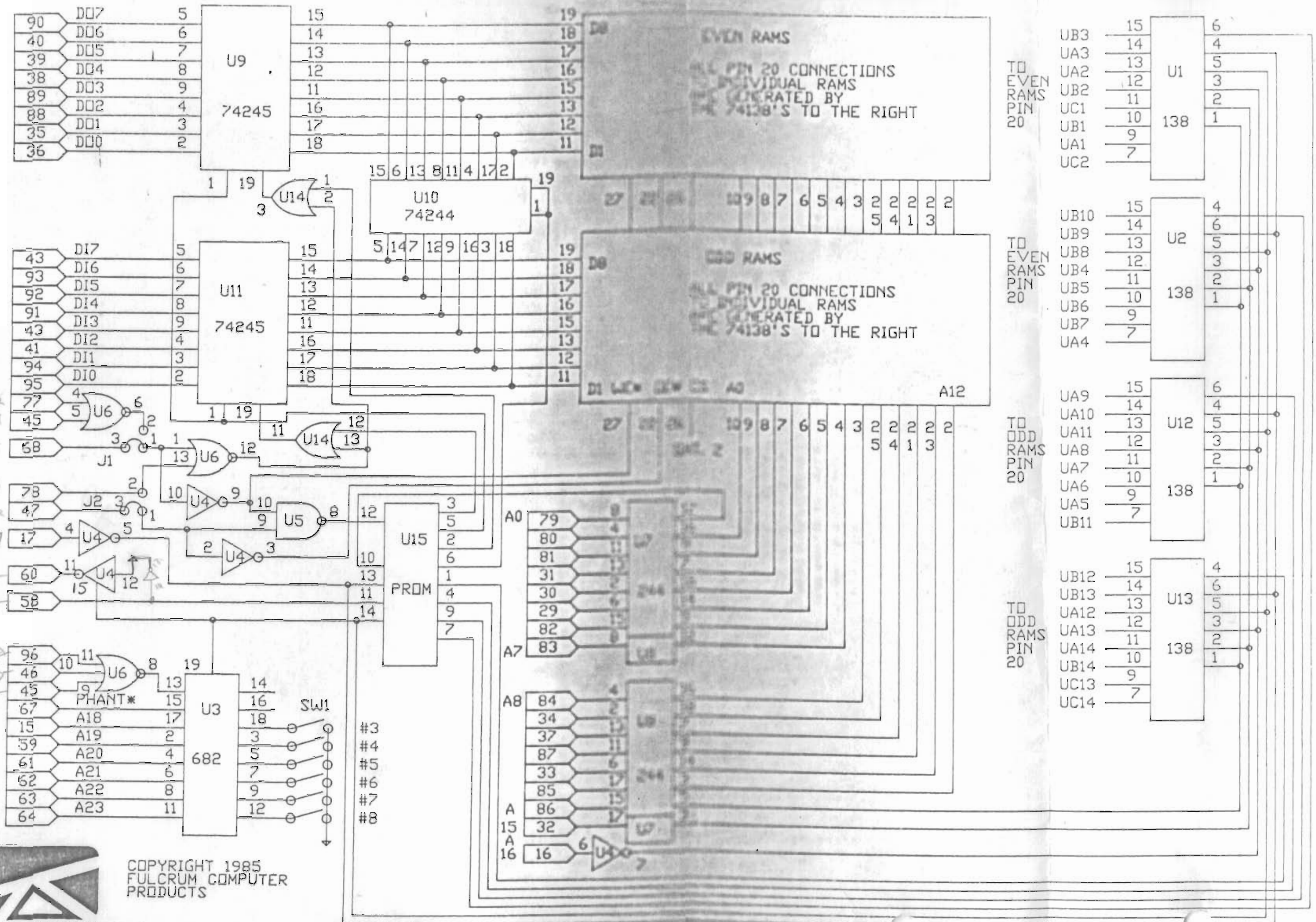
address/state				data							
13	12	11	10	1	2	3	4	5	6	7	8
A17*	RD*	IORQ	A0	O-CS*	DOEN*	DIEN*	O-CS	245DIR	244EN*	E-CS	E-CS*
0	0	0	0	1	1	1	0	1	1	0	1
0	0	0	1	1	0	0	1	0	1	1	1
0	0	1	0	1	0	0	1	0	1	1	1
0	0	1	1	1	1	0	0	0	0	1	1
0	1	0	0	1	1	0	1	0	1	0	1
0	1	0	1	1	0	0	1	1	1	1	1
0	1	1	0	1	0	0	1	1	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1	0	0
1	0	1	0	1	1	0	0	0	0	0	0
1	0	1	1	0	1	0	0	0	1	0	1
1	1	0	0	0	0	0	0	1	1	0	0
1	1	0	1	0	0	0	0	1	1	0	0
1	1	1	0	1	0	1	0	1	1	0	0
1	1	1	1	0	0	1	0	1	0	0	1

address/state			Operation
0	0000	B7	--
1	0001	E9	16 bit read
2	0010	E9	16 bit read
3	0011	C3	8 bit read , even byte
4	0100	AB	8 bit read , odd byte
5	0101	F9	16 bit write
6	0110	F9	16 bit write
7	0111	F5	8 bit write, even byte
8	1000	20	16 bit read
9	1001	20	16 bit read
10	1010	03	8 bit read , even byte
11	1011	A2	8 bit read , odd byte
12	1100	30	16 bit write
13	1101	30	16 bit write
14	1110	35	8 bit write, even byte
15	1111	94	8 bit write, odd byte

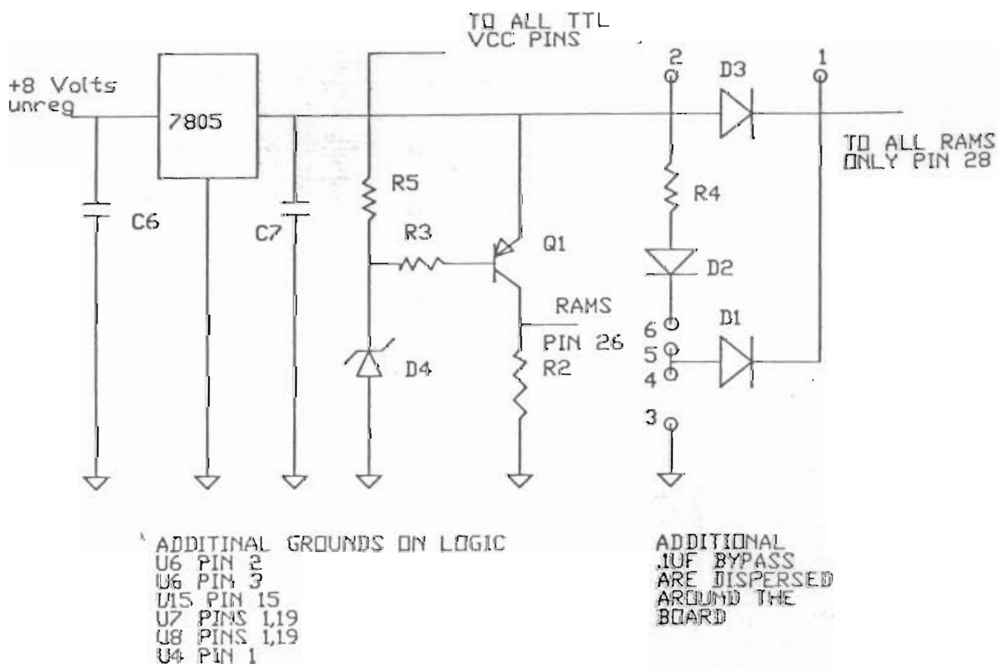
6.4 Component List

Designation	Type	Description
U1-2,U12-13	74LS138	1 of 8 decoder
U3	74LS682	8-input comparator
U4	74LS368	Quad buffer
U5	74LS00	Quad 2-input NAND gate
U6	74LS27	Triple 3-input NOR gate
U7-8	74LS244, or 74LS240	Octal buffer
U10	74LS244	Octal buffer
U9,U11	74LS245	Octal bi-directional buffer
U14	74LS32	Quad 2-input OR gate
U15	TBP18S030N	32x8 PROM (Alt. 74S288)
UA1-UC14	HM6264LP-12	8192 x 8 SRAM, 120 ns
C1-5	0.1u	Bypass capacitor, glass
C6-7	0.47u/35v	Bypass capacitor, tantalum
Q1	2N3906, PNP	Transistor
D1-2	1N3600	Switching diode
D3		Schottky barrier diode
D4	1N4372A,	4.3v zener
VR1	7805,	5v regulator
R1		
R2	5K, 0.25w	resistor
R3	1k, 0.25w	resistor
R4-5	100 ohm, 0.25w	resistor


OMNI256
COPYRIGHT 1985
REV. A
6264
U15
82S123
U12
138
U13
138
U14
32
C5
U11
245
C4
U10
244
U9
245
U8
244
C3
U7
244
U6
27
C2
U5
08
J2
J1
U4
368
U3
682
SW1
C1
138
U1
C7
C6
D1
D2
D3
D4
R1
R2
R3
Q1
50
40
30
20
10



FULCRUM
COMPUTER PRODUCTS


TO ALL TTL
VCC PINS
+8 Volts
unreg
7805
C6
C7
R5
R3
Q1
D4
RAMS
PIN 26
R2
2
D3
1
TO ALL RAMS
ONLY PIN 28
R4
D2
D1
6
5
4
3
ADDITINAL GROUNDS ON LOGIC
U6 PIN 2
U6 PIN 3
U15 PIN 15
U7 PINS 1,19
U8 PINS 1,19
U4 PIN 1
ADDITIONAL
.1UF BYPASS
ARE DISPERSED
AROUND THE
BOARD